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Design and characterization of a modular GaN-based power stage for automotive applications

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A mia madre,
la stella che illumina il mio cammino.

Abstract

This thesis presents the design and characterization of a modular power stage using Gallium Nitride (GaN) transistors for automotive three-phase inverter applications. The project was carried out as an internship at Ideas & Motion s.r.l, in collaboration with the Politecnico di Torino, with the aim of creating an efficient, compact and reliable inverter system suitable for high-power demands in electric vehicles. GaN technology was selected due to its high voltage capability, fast switching speed and superior efficiency compared to traditional silicon-based systems, making it ideal for the rigorous requirements of automotive power electronics. The work begins by examining the technological and environmental motivations driving the electrification of transportation, as well as the fundamental principles of power conversion and the advantages of wide-bandgap devices. A detailed breakdown of the GaN-based inverter follows, describing the individual subsystems and their integration within overall design. The focus then shifts to the design process, covering critical decisions in component selection, circuit architecture and PCB layout. Finally, the testing phase, where the inverter's performance is validated, is discussed to assess its operational stability, efficiency and suitability for automotive applications. This study combines theoretical analysis with practical implementation to showcase the potential of GaN technology to meet the stringent demands of automotive systems. The results highlight the inverter's capability to manage efficiently high voltage and high current levels, contributing to the broader transition towards sustainable electric mobility.

Contents

Chapter 1

Introduction

Inverters are a core technology in power electronics, as they convert direct current (DC) to alternating current (AC). This task is very important in numerous applications, including industrial power systems, and is becoming even more pertinent in the newly emerging areas of electric vehicles (EVs) and hybrid electric vehicles (HEVs). The importance of inverters has only grown in modern energy systems due to the greater emphasis on energy efficiency and the global move towards sustainable technologies. In particular, electric mobility has become a prime target for innovation, owing to the pressing need to lower greenhouse gas emissions and lessen reliance on fossil fuels. Therefore, the advancement of high-performance inverters has become a key pursuit in meeting the objectives of compactness, efficiency and reliability of electric(s) vehicle (EV) and hybrid electric vehicle (HEV) powertrains.

Inverter for EV and HEV applications must meet several demanding requirements. These consist of matching high efficiency over a wide range of loads, high energy density for the compaction of the power supply device, and safe operation under severe thermal and electrical stress. In addition, new opportunities in next-generation inverters designed with advanced semiconductor materials have been emerging. However, these benefits come with new challenges in terms of topology design, thermal management and control strategies that need to be overcome to meet their potential

For this reason, the research community and industry standardize is focusing on Key Performance Indicators (KPIs) to evaluate and compare inverter designs. These measurements provide a consistent basis to quantify and compare the performance of inverters with respect to power, efficiency, size and reliability. Among these, the significant are: **power density** (kW/kg), which is a measurement of how much power can be delivered in relation to the physical weight of the inverter; and **specific power** (kW/l), which measures power output relative to package volume, such as when comparing designs and technologies.

Power density, measures how much power an inverter can produce compared to its mass. This is especially critical in applications like EVs and HEVs, as reducing the mass of a single component can directly improve system efficiency and range. Reducing the mass of power electronics allows manufacturers to optimize energy consumption and recover available payload volume for other key components such as batteries or structure reinforcements.

On the other hand, specific power measures the amount of power that an inverter can provide for a specific amount of physical space. This metric indicates the compactness of the design, which is a crucial aspect in automotive applications which where the space is very limited. Key to achieving these ambitious goals will be using a higher degree of specific power to allow the engineer to integrate the inverter easily into vehicle architectures without altering the design to a great extent or needing major changes to package bulky power electronics. One of the main challenges is achieving a compromise between high specific power and effective thermal management, as more compact designs can put more strain on heat dissipation.

Table 1: Timeline of inverter technologies highlighting advancements in specific power and power density [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]

Year	Author	Title	Power Density, kW/kg	Specific Power, kW/l
2016	Yamagichi	Design and Evaluation of SiC-Based High Power Density Inverter, 70kW/liter, 50kW/kg	50	70
2016	Cadillac CT6 PHEV	Compact and High Power Inverter for the Cadillac CT6 Rear Wheel Drive PHEV	16,0	22,6
2016	BMW i3		18,5	14,1
2017	Opel Ampera		15,6	19,2
2017	Chevrolet Bolt		15,6	19,2
2017	Wijenayake	Design of a 250 kW, 1200 V SiC MOSFET-Based Three-Phase Inverter by Considering a Subsystem Level Design Optimization Approach	15,6	
2018	Tesla Model 3		30,0	30
2019	Audi E-Tron		19,0	24
2020	Van Adamnson	An 800-V High-Density Traction Inverter – Electro-Thermal Characterization and Low-Inductance PCB Bussing Design		85,7
2020	Wu	An Optimized Silicon Carbide based 2×250 kW Dual Inverter for Traction Applications	60	
2021	Sato	High power density inverter utilizing SiC MOSFET and interstitial via hole PCB for motor drive system	81	
2022	Al hamoud	A High-Density 200-kW All Silicon Carbide Three-Phase Inverter for Traction Applications		43,0
2023	Zhao	Design and Optimization of 2×211-kW SiC-Based Aircraft Propulsion Inverter System	19,5	
2024	Forte	High Power-Density Design Based on WBG GaN Devices for Three-Phase Motor Drives		59,6
2024	Zhen	A Very High- Power Density Multilevel Inverter Using Silicon Carbide (SiC) Commercial-Off- The-Shelf (COTS) Parts	60,0	
2025	U.S DRIVE Partnership	Electrical and electronics techical team roadmap		100,0

These combined metrics offer a comprehensive approach to ensure that inverter designs are efficient and practical. They are important because they offer the ability to act as anchor points for literation comparison of state of the art systems and also to act as a basis for the creation of more advanced systems that are better performing and better optimizing. It is fundamentally difficult to improve both power density and specific power, as this requires a delicate balancing act between material characteristics, circuit topologies, thermal management, and system reliability. Optimizing these platforms is a truly multidisciplinary endeavor, combining improvements in wide bandgap semiconductors, cooling methods, and packaging techniques, solidifying their place in the future of power electronics.

The accompanying graphs (Figure 1 and Figure 2) illustrate the trends in literature of these key performance indicators for three-phase inverters as reported in the Table 1.

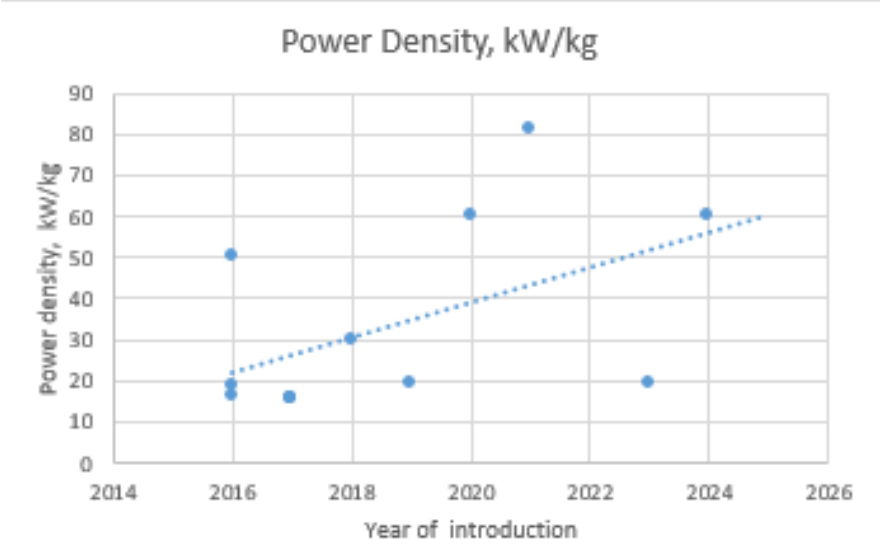


Figure 1: Power density trend of inverters

Power density has improved steadily over the years as well, with modern inverter designs now approaching 80 kW/kg. These impressive advances show that the industry can manage to substantially decrease the mass of inverter systems while keeping or raising their power output. Central to this progress has been the adoption of new semiconductor materials such as gallium nitride (GaN) and silicon carbide (SiC), which boast superior properties compared with conventional silicon-based technologies. These wide bandgap (WBG) materials permit higher efficiency, lower switching, lower conduction losses and smaller designs, resulting in lighter and more efficient inverter designs.

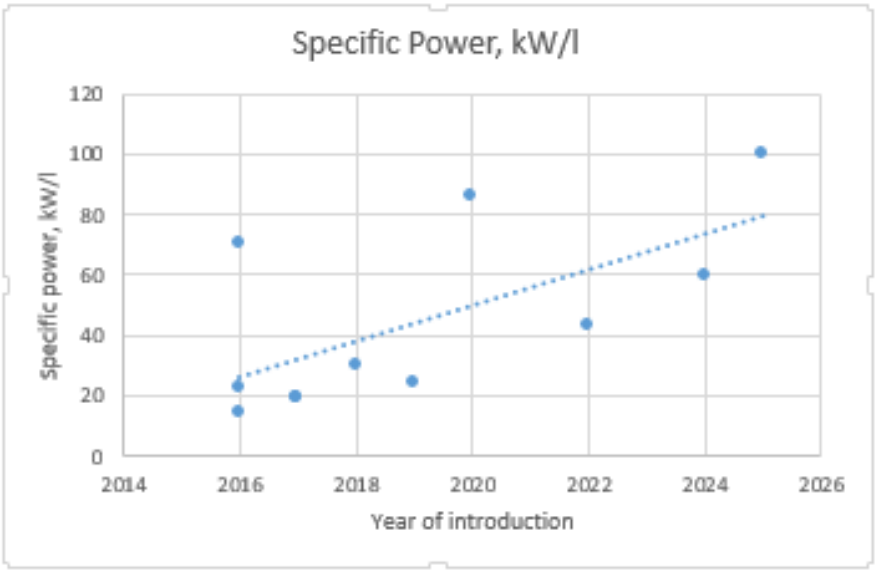


Figure 2: Specific power trend of inverters

Likewise, specific power has made significant strides with the most recent inverters aimed for 100 kW/l by 2025. Apart from the new materials, sophisticated cooling solutions have been crucial in reaching these specific power values. In regard to more compact designs operating on high power density, we have successfully been able to manage the added heat with the help of liquid cooling systems, integrated heat sinks, and better thermal interfaces. Through innovative thermal management strategies, inverters can be made smaller while still operating smoothly in spite of demanding conditions, which is necessarily the case with electric and hybrid vehicle applications.

In conclusion, this introduction indicates that power density and specific power are extremely important criteria to rate three-phase inverters for EV and HEV applications. The aim of this thesis is to contribute to the development of inverter technology with GaN-based designs that extend beyond conventional levels in terms of efficiency, size and reliability. The upcoming chapters are focused on the theory behind, the design and experimental implementation of the introduced inverter and will prepare the grounds for comparing it with the state of art products.

Chapter 2

Electrification of transportation

Transportation electrification has become one of the most critical elements of the global energy transition due to the requirement to decarbonize mobility, which accounts for roughly 25% of global CO_2 emissions. In response to this challenge, countries across the planet are implementing policies to simultaneously curb the number of internal combustion engine (ICE) vehicles on the road and bring about the adoption of EVs in the hopes of reaching climate goals. According to the International Energy Agency's Global EV Outlook 2024 report, worldwide EV sales are set to surpass 17 million units in 2024, more than 20% of total car sales. This is a major increase from earlier years, signalling that EVs are starting to transition from being niche products to something which has become more mainstream in many markets, particularly China, Europe and USA. China is the world leader in EV adoption, with more than 60% of electric car sales in 2023, thanks to strong government policies and heavy investments in EV infrastructure and manufacturing. Europe also sees strong growth, expecting electric cars to be 25% of new car sales by 2024, while the U.S. will see that number climb over 11% also in 2024. Transmission to these territories is prodded by severe CO2 outflow guidelines and systems that persuade shoppers and producers to embrace electric mobility. The European Union intends to prohibit the sale of new gasoline and diesel cars by 2035, while the U.S. Inflation Reduction Act (IRA) offers massive subsidies for EV manufacturers and buyers, driving local production and adoption. Nevertheless, growth in EVs in developing markets is slower. Although EV sales have surged in countries such as Vietnam (up 15%) and Thailand (up 10%), many developing countries still have hurdles to overcome, including inadequate charging infrastructure and high upfront costs. For this to enable global electrification to succeed, these markets will require a more targeted policy approach and investment [12].

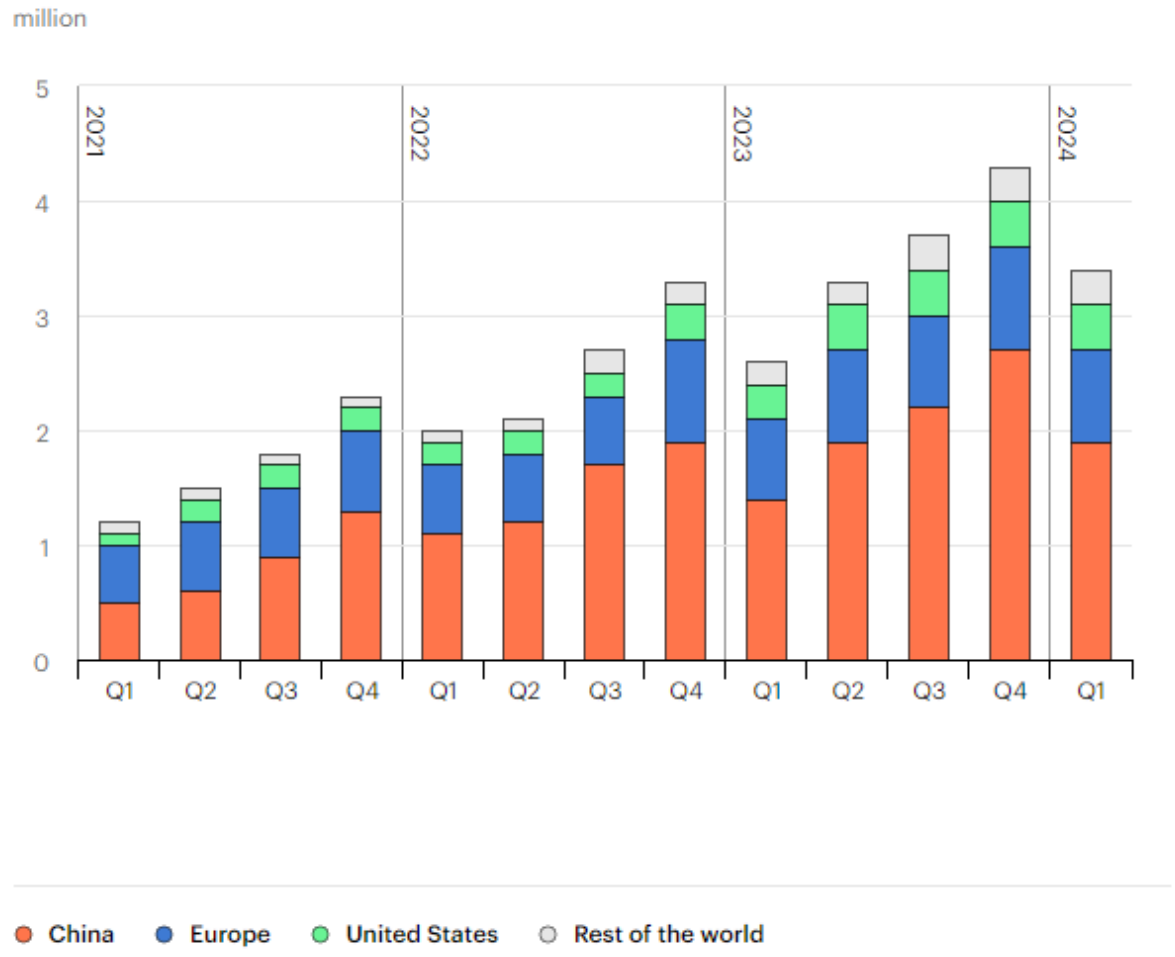


Figure 3: Quarterly electric car sales by region, 2021-2024 [12]

2.1 Motivations

Environmental, economic and technological factors all drive the switch to EVs. These factors underscore the urgent need to decarbonize transportation, improve energy efficiency, enhance energy security and generate new economic opportunities in a period of growing environmental consciousness. On the social front, electrifying the transport system, particularly in urban areas, can lead to a better quality of life, evidenced through reduced noise pollution and improved air quality. This leads to healthier living conditions and reduced public health costs related to respiratory and cardiovascular illnesses.

One of the best reasons to electrify transportation is to decrease the level of greenhouse gases, particularly carbon dioxide (CO_2), and other harmful air pollutants, particularly nitrogen oxides (NOX) and particulate matter (PM10 and PM2. 5). Internal combustion engine vehicles are major contributors to these emissions, worsening climate change and contributing to poor urban air quality.

Electric vehicles, on the other hand, do not emit any tailpipe emissions, thus directly removing local air pollutants. The one caveat is the indirect emissions generated by using electricity to charge the vehicles. Where energy systems produce electricity from renewables or low-carbon sources — nuclear, wind or solar power — the emissions reduction is significant. It also widely recognised that the greater the amount of renewable energy being fed into the grid, the more the environmental benefits of EVs would increase, even in countries that rely heavily on fossil fuel generation. Another key motive is better public health: local air pollution is expected to decrease significantly when shifting to electrification, as studies indicate that poor air quality leads to millions of premature deaths each year worldwide [13].

The improvement in energy efficiency is another strong reason for the electrification of transportation. Electric vehicles are inherently more efficient than internal combustion vehicles are. ICE vehicles, on the other hand, convert less than 30% of the fuel energy in gasoline into motion [14], but electric motors can achieve efficiencies greater than 70% [14]. That inefficiency gap is what makes EVs use drastically less energy than traditional vehicles for the same distance travelled. In addition, due to regenerative braking in electric vehicles, energy that would otherwise be wasted when slowing down can instead be reclaimed, improving the efficiency of electric vehicles even more. The reduction in required energy per unit output is all pertinent in these times of rising global energy demands and an imperative to optimise available resources. In the urban areas, the replacement of ICE vehicles with electric vehicles (e.g., buses and trams) can decrease the primary energy demand drastically. The European Commission indicated that electrified public transport systems also consume 20 to 30% less energy than conventional systems [15].

Electrifying transportation is an important part of decreasing global reliance on fossil fuels. In this moment, most chime in the dynamics of global transport depends on oil, which is a finite resource, unreliable price fluctuations and geopolitical uncertainties. Such a dependency makes the economies susceptible of energy crises and trade imbalance. Electrification provides an opportunity to de-risk the energy sources used in the transportation sector by increasing reliance on renewables such as solar, wind and hydropower. This not only lessens dependence on oil but also stabilizes international energy markets. Lower oil demand also bodes well for national energy security since states do not have to rely as much on oil-exporting countries or weather the risk of conflict or political turmoil in those areas. If current trends continue, electrification could reduce global oil demand by close to 2.5 million barrels per day by 2030 [16].

In addition to environmental benefits, transportation electrification offers to unlock numerous economic and social opportunities. At a macroeconomic level, the movement towards EVs can lead to new industries and job opportunities in

sectors such as EV manufacturing, battery production and charging infrastructure development. Long-term cost decreases in energy are driven by the technological innovation related to electrification, which can also help accelerate the transition toward a more green and sustainable economy. The initial costs are higher for EVs, but their operating costs are lower because of less maintenance and cheaper electricity than gas. According to a recent Gartner report, It is expected that by 2027 EVs will be cheaper to produce relative to a comparable ICE, making it even more attractive to consumers [17].

2.2 Power conversion

Power conversion is a necessary component of our current electronics and electrical engineering that allows electrical power to be transformed from one form to another. DC (Direct current) and AC (Alternating current) are the two basic forms of electrical power and it is through power conversion that devices are able to consume, store or generate the proper form of power when they require it. Further, the conventional power conversion devices have more than one power conversion mode, and the operation of these modes is decoupled on an instantaneous basis through storage means (capacitors and inductors). As such, a converter is the elementary building block of a power electronics system [18].

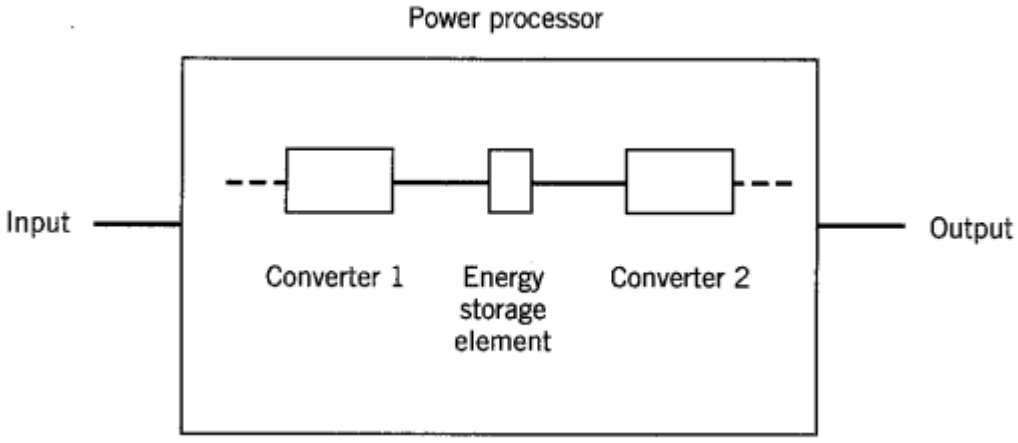
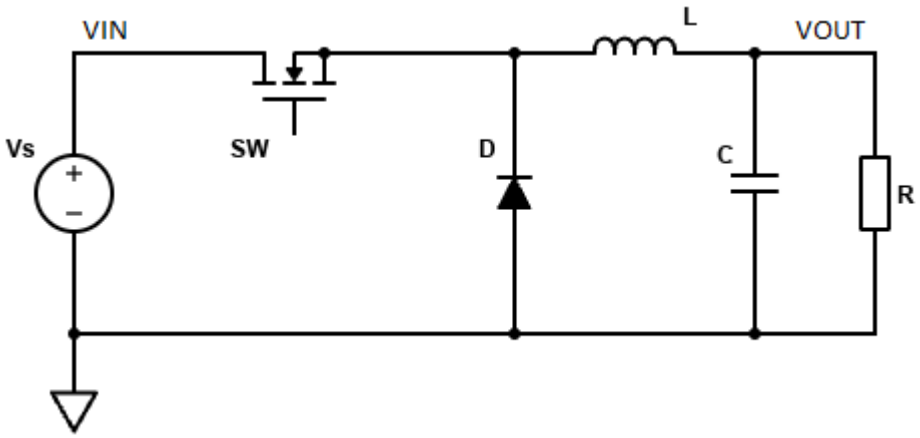


Figure 4: Power processor block diagram [18].

Power converters are broadly classified based on the types of power they convert and the techniques they use to achieve conversion. The three most common types are:

- **DC-to-DC converters**: Also known as Choppers or Chopper, are circuits that convert source direct current to a different voltage level. They are often used in applications that require a stable voltage, such as a battery-powered device, or to ensure acceptable voltage levels in renewable energy systems. There are lots of topologies but the basic are:

    1. Step-down (Buck) converters: a Buck converter converts a higher DC input voltage to where the output is a lower DC voltage. It is frequently used in power supply unit to deliver stable voltages to microprocessor and other components. Basically, a buck converter controls the amount of energy stored in an inductor by switching a transistor ON and OFF, and then releases this power to a load at lower voltage.



2.

Figure 5: Buck converter

    3. Step-up (Boost) converters: on the other hand, a Boost converter steps up a DC input voltage to a higher DC output voltage. These converters are typically used in applications such as solar power systems, where they step up the voltage from a solar panel to a level sufficient for charging batteries or being fed into the grid.

    4. Buck-Boost converters: these converters are such type where input voltage can be increased or decreased, as per requirements. The regulator will have a DC input voltage and will output a DC voltage with an approximately equal magnitude but opposite polarity. They are flexible and serve effective in battery-operated equipment where the battery voltage changes, however, constant output voltage is required [19].

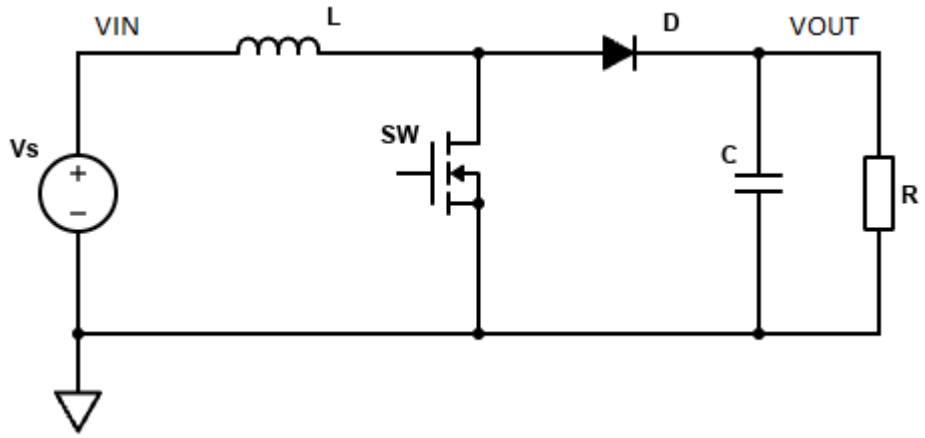


Figure 6: Boost converter

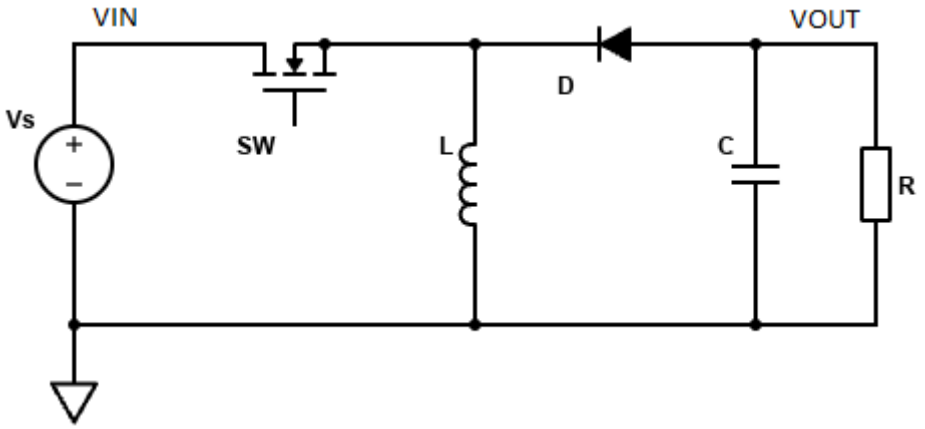


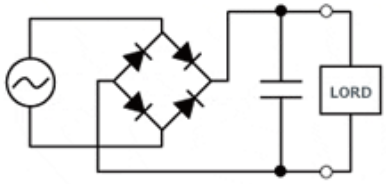
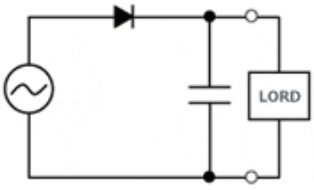
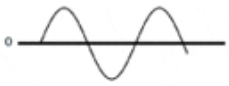
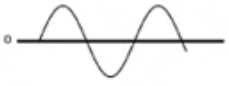
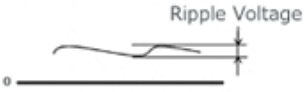
Figure 7: Buck-Boost converter

- **AC-to-DC converters**: Also known as Rectifiers, are used to convert alternating current into direct current. These are commonly found in power supplies for electronic devices, where AC from the grid is converted to DC for use by electronic circuits. We distinguish two basic types:

    1. Half-Wave rectifiers: a Half-Wave rectifier passes only one half of the AC waveform and blocks the other half. This creates a pulsing DC that is usually smoothed by use of capacitors for stable operation.

    2. Full-Wave rectifiers: a Full-Wave rectifier use both halves of the AC waveform providing a smoother DC output. These full-wave rectifiers consist of a diode bridge or center-tapped transformer. Filter circuits are widely connected to both forms of rectifiers to reduce ripple and ensure a cleaner DC output, which is a vital need for driving sensitive electronic components [20].

Table 2: Full-Wave and Half-Wave rectification [20]

	Full-Wave Rectification	Half-Wave Rectification
Circuit Configuration		
Input Voltage Waveform		
Voltage Waveform After Rectification		
Voltage Waveform After Rectification Smoothing		

- **DC-to-AC converters (inverters)**: The primary purpose of static power converters is to generate an AC output waveform from a DC power source. For sinusoidal AC outputs, it is essential to control the magnitude, frequency and phase of the waveform. Inverters are widely used in renewable energy systems, uninterruptible power supplies (UPS) and electric vehicles to convert the DC power stored in batteries into AC power suitable for driving motors or powering appliances.

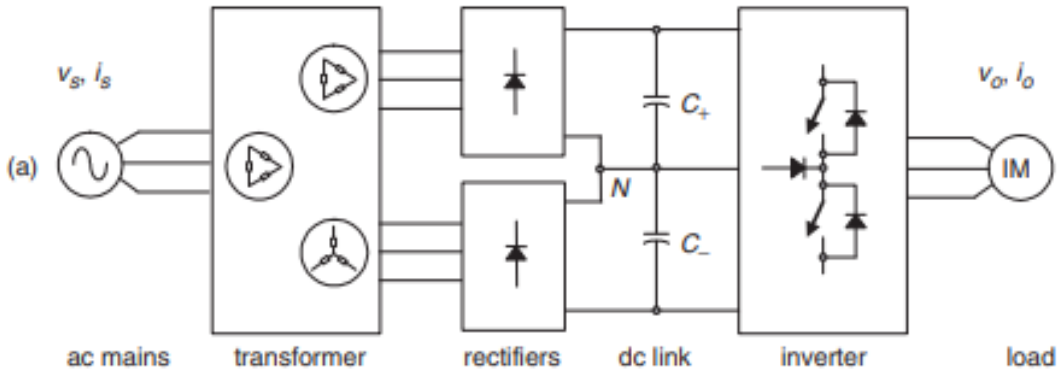


Figure 8: Electrical power conversion topology [21].

They use a series of switching components and modulation methods to generate an AC waveform from a DC input. The devices with the highest incidence factor in an inverter switching are Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and Insulated Gate Bipolar Transistors (IGBTs), which provide a variety of pros and cons in speed, efficiency and power handling.

Depending on the class of the DC input source, these converters are primarily classified into two categories as Voltage Source Inverters (VSI) and Current Source Inverters (CSI). While there are three VSI based topologies, they are the most used type since their nature is already combined as they are a voltage source, which is needed for many industrial applications. CSIs are still extensively used in medium-voltage industrial applications, especially where high-quality voltage waveform are required [21].

Inverters can be also classified based on multiple factors, including the waveform they produce, the number of phases they support and their application. For the phase, we have two main categories:

1. Single-Phase Inverters: Typically used in residential and light commercial applications. They convert DC into a single-phase AC output, which is suitable for powering household appliances, lighting and small loads.
2. Three-Phase Inverters: Commonly used in industrial applications, three-phase inverters generate AC power in three phases, which is essential for driving large motors, heavy machinery and other high-power equipment.

The output voltage can harmonics along with ripples and in best cases they are very small and hence the output waveform ideally should be a pure sine wave. DC power is drawn from the input power source by the inverter only when the load is connected to the supply. Hence, the input current is not pure DC and consists of harmonic components. Typically the performance of an inverter is evaluated on various parameters:

1. Harmonic factor of *n*th harmonic (HF_n): is a measure of individual harmonic contribution.
2. Total harmonic distortion (THD): is a measure of closeness in shape between a waveform and its fundamental component.
3. Distortion factor (DF): THD gives the total harmonic content, but it does not indicate the level of each harmonic component. If a filter is used at the output of inverters, the higher order harmonics would be attenuated more effectively. Therefore, a

knowledge of both the frequency and magnitude of each harmonic is important. The DF indicates the amount of harmonic distortion that remains in a particular waveform after the harmonics of that waveform have been subjected to a second-order attenuation. Thus, DF is a measure of effectiveness in reducing unwanted harmonics without having to specify the values of a second-order load filter.

4. Lowest order harmonic (LOH): the LOH is that harmonic component whose frequency is closest to the fundamental one, and its amplitude is greater than or equal to 3% of the fundamental component [22].

Furthermore, modulation techniques play a vital role in controlling inverter performance, demanding high efficiency and accurate and high performance output characteristics. These approaches manage the frequency, amplitude and phase of the output voltage or current by modulating the inverter's switching patterns, encapsulating the exact requirements of different applications, whether it is motor drives or renewable energy systems. Pulse Width Modulation (PWM) is one of the most commonly used modulation technique in inverter and the devices with PWM modulation are called as PWM inverters. PWM inverters removes lower order harmonics and reduce the THD content at output AC voltage. They also reduce the need for filters. The most popular modulation types used in inverters are:

1. Single pulse modulation: this modulation technique consists of one pulse per half-cycle, and the width of the pulse varies from 0 to π. By varying the pulse width, the output voltage is controlled.

2. Multiple pulse modulation: this modulation scheme is an extension of single pulse modulation, where several equidistant pulses are present per half cycle. The pulse width is equal in multiple pulse modulation.

3. Sinusoidal pulse width modulation : this is a type of multiple pulse modulation, where several pulses are present in each half-cycle. The pulse width is the sinusoidal function of the angular position of the pulse in a cycle.

4. Space vector modulation: the space vector modulation scheme is commonly used in inverters due to its ease of implementation. It is frequently employed in multilevel inverters [23].

2.3 Wide band-gap devices

A crucial step toward achieving an energy-efficient world lies in the adoption of innovative materials, such as wide band-gap (WBG) semiconductors. Energy consumption and management in buildings are heavily reliant on power electronic converters and the monitoring of indoor conditions. It is worth noting that much of the electrical power generated is eventually used only after the electrical power has been transformed several times into different currents, all of which is very wasteful and performed by power electronic converters. Semiconductors are vital for the next generation of key technologies, such as electronics, optoelectronics, communications, computing and sensing. Semiconductor device and switching frequency selection play a significant role in power converter efficiency. Semiconductor devices in power electronics converter systems play a major role in power losses during high current conduction and switching.

Considerably, high switching frequencies are required for WBG semiconductor materials to reduce switching loss and improve the power density of the converters. Therefore, power electronics innovations are crucial to minimizing the power losses in power conversion. Indeed, WBG semiconductor power devices can optimize electrical energy conversion without compromising performance and efficiency of power converters. WBG-based devices can further miniaturize power electronic components with resultant improvements in reducing system or component level costs; performance; and reliability. One of the few properties that dictate the electrical and optical behaviours of a semiconductor is the bandgap, the most important parameter when it comes to identifying a WBG semiconductor. This quantity is defined as the energy barrier which electrons have to cross to go from the valence band to the conduction band. In fact, the ferromagnetic behaviour of semiconducting materials plays an important role for the choice of power components especially in terms of energy performance, hysteresis and eddy current loss. WBG semiconductor materials have wider bandgaps (2–4 eV) compared to silicon (1–1.5 eV), offering higher power efficiency, lower overall costs, reduced size and weight, and lower energy consumption. The use of WBG material translates directly into semiconductor devices operating at high temperatures, which may cause problems for traditional silicon semiconductors with smaller bandgaps. The temperature range of semiconductor power devices is enhanced with an increased bandgap. WBG also allows electronic devices made from these materials to endure higher heat and radiation without deteriorating their electrical properties. They also show the fast switching speed, low on-state resistance, as well as higher temperature and voltage capabilities. Quicker and lower switching loss means smaller passive components and heatsinks with improved power density.

WBG semiconductor power devices outperform silicon-based devices in demanding conditions. When utilizing energy storage systems, appropriate power converters are necessary to manage energy flow during charging and discharging to maximize their full potential. Thus, the research on efficient semiconductor power electronics is of great importance to maximum energy usage of the stored energy in batteries, supercapacitors, etc [24].

Thanks to decades of developments in fabrication processes, material supply, large-scale manufacturing, and drastically reduced costs, silicon is still the element of choice for most power semiconductor device applications. It is primarily due to its technological maturity and the widespread accessibility of materials. But silicon-based devices cannot meet the advanced requirements of modern power electronics for applications with a high power density or high-voltage devices, operating at frequencies and temperatures higher than 150°C. Meanwhile, it is thought that alternatives, such as materials such as silicon carbide or gallium nitride, hold greater long term promise. Their efficiency, as well as availability of raw materials and their technologies' maturity levels, makes them attractive Contributor. Especially for power electronics, from the perspectives of device manufacturers, SiC and GaN are the most promising WBG semiconductor materials. One of the major advantages besides increasing productivity in power applications is that WBG power devices are most capable of operating at high temperatures. They provide enhanced blocking voltage, current carrying capability, and can operate at higher frequencies, power levels, and voltages. GaN-based power devices as core devices in the power conversion industry, which is essential for the operations of smartphones, computers, battery chargers, automotive systems, lighting and photovoltaics. This WBG technology provides best achievable designs for passive components, converter topologies, and thermal management when integrated into a power electronics systems. The benefits of WBG power devices make them impactful in an array of applications. So they are also good in high-power applications such as electric vehicles and other areas as they have moved beyond the limits of silicone and are designed for optimal performance in harsh environments, allowing them to be smaller, lighter, and cheaper [24].

Table 3: Material properties of Si, GaN and SiC

Parameter		**Silicon**	**GaN**	**SiC**
Band Gap (E_g)	[eV]	1.12	3.39	3.26
Critical Field (E_{crit})	[MV/cm]	0.23	3.3	2.2
Electron Mobility (μ_n)	[cm^2/V·s]	1400	1500	950
Permittivity (ε_r)		11.8	9	9.7
Thermal conductivity (λ)	[W/cm·K]	1.5	1.3	3.8

Band gap of a semiconductor is related to the strength of the chemical bonds between the atoms in the lattice. These stronger bonds mean that it is harder for an electron to jump from one site to the next. Among the many consequences are lower intrinsic leakage currents and higher operating temperatures for higher band gap semiconductors. The stronger chemical bonds that cause the wider band gap also result in a higher critical electric field needed to initiate impact ionization, thus causing avalanche breakdown. The voltage at which a device breaks down can be approximated with the formula [25] :

$$V_{BR} = {}^{1}/_{2}\ w_{drift} \cdot E_{crit} \tag{1}$$

The breakdown voltage of a device, therefore, is proportional to the width of the drift region. In the case of SiC and GaN, the drift region can be 10 times smaller than in silicon for the same breakdown voltage. In order to support this electric field, there need to be carriers in the drift region that are depleted away at the point where the device reaches the critical field. This is where there is a huge gain in devices with high critical fields. The number of electrons (assuming an N-type semiconductor) between the two terminals can be calculated using Poison's equation [25]:

$$q \cdot N_D = \varepsilon_0 \varepsilon_r \cdot \frac{E_{crit}}{w_{drift}} \tag{2}$$

In this equation, q is the charge of the electron, N_D is the total number of electrons in the volume, ε_0 is the permittivity of a vacuum measured in farads per meter and ε_r is the relative permittivity. It can be seen that if the critical field of the crystal is 10 times higher, the electrical terminals can be 10 times closer together. Therefore, the number of electrons in the drift region can be 100 times greater. This is the basis for the ability of GaN and SiC to outperform silicon in power conversion [25].

The theoretical on-resistance of this majority-carrier device is therefore [25]:

$$R_{DS(On)} = \frac{w_{drift}}{q \cdot \mu_n \cdot N_D} \tag{3}$$

Combining Equation 1, Equation 2 and Equation 3, we obtain:

$$R_{DS(on)} = 4 \cdot \frac{V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot E_{crit}^3} \quad (4)$$

Where μ_n is the mobility of electrons [14]. The material dependent parameters of the Equation 4, such as relative permittivity ε_r, electron mobility μ_n and critical field E_{crit} are included into the so called Baliga's figure of merit (BFoM) for power devices. Therefore, basically the BFoM is a measure for the material dependence of the on-resistance of unipolar devices [26].

High-voltage (HV) power semiconductor switches play vital role in any power conversion system. Silicon-based insulated gate bipolar transistors (IGBTs) are widely used because they are now mature, and there is no alternative available. While incremental efficiency improvements can be made by using Si IGBTs in conjunction with SiC diodes, the resulting gains are marginal. Si IGBTs exhibit intrinsic limitations in operating frequency, switching speed, and high temperature operation, in addition to poor performance at low current. Furthermore, in high-frequency applications such as AC-to-DC power factor correction (PFC) and DC-to-DC power conversion, Si super-junction (SJ) technology is dominant. Si-based devices, on the other hand, are constrained in size or cost owing to limited material capabilities at high frequencies. This is mainly caused by switching crossover losses, conduction losses and reverse recovery losses. On the other hand, wide bandgap (WBG) materials, due to their fast turn-on and turn-off switching capabilities, and low conduction losses, help to overcome reverse recovery loss and also have low switching crossover losses. Higher critical electric fields and electron mobility in WBG materials yield lower on-state resistance for high-voltage applications, leading to superior switching performance. The WBG devices are now coming to market with great potential, addressing many of the innate limitations of Si IGBT and Si SJ devices [26].

GaN FETs come in two base configurations: enhancement mode (E-mode) or depletion mode (D-mode) devices. In power conversion applications, D-mode devices are disadvantageous since, during the start-up of a power converter, the power devices must be pre-biased negatively. Failure to apply this negative bias first will cause a short circuit. A device that was E-mode would not have this limitation. •With no bias on the gate, an E-mode will be in the OFF mode and will not conduct current until a positive voltage is applied to the gate One approach to designing a single-chip enhancement-mode GaN transistor is to stack an enhancement-mode silicon MOSFET in series with a depletion-mode HEMT (High Electron Mobility Transistor) device. The depletion-mode GaN transistor gate voltage drops to near-zero volts, and it turns on, which in this circuit turns the MOSFET on with a positive voltage on the gate. The current is able to flow

through the depletion-mode GaN HEMT and the MOSFET (in series with the GaN HEMT). The application of a negative voltage between the depletion-mode GaN transistor gate and its source electrode turns the GaN device off when the voltage on the MOS gate is removed. This kind of solution for an enhancement-mode GaN system is suitable when the on-resistance of the GaN transistor is relatively higher than that of the low voltage silicon MOSFET. Because on-resistance grows with device breakdown voltage, cascode solutions will work best if the GaN HEMT is high voltage and the MOSFET is quite low voltage. E-mode gates are stable, but leakage currents in E-mode gates must be analyzed carefully for better performance. E-mode devices for high-voltage, high-power applications need complex drive circuitry. These applications require high gate threshold voltage and stable gate drive to prevent gate bounce and shoot-through, conditions which cannot be achieved with current E-mode technology. The cascode architecture, as an additional precaution, also ensures that the gate structure doesn't sacrifice the level of reliability that is required by automotive applications. This dependability provides a powerful and flexible tool for the high-performance power electronics sector [27].

Chapter 3

Study of a GaN-based inverter power stage

The Introduction of Gallium Nitride transistors in power electronics has significantly changed design and characteristics of modern inverters. The electrical performance advantages of GaN-based transistors— including higher breakdown voltages, improved switching speeds, and lower conduction losses — have led to heightened market acceptance of enhancement-mode devices, which are gradually superseding conventional Silicon MOSFETs in a wide range of applications. These features make GaN transistors ideal for applications where efficiency, size, and power density are key, such as electric vehicles, renewable energy systems, telecommunications, and industrial motor drives.

One of the most significant uses of GaN technology is for the design of inverters responsible for converting DC power into AC power. Inverters design contribute to various system architectures like solar power plants, EVs, UPS, etc., demanding ever-increasing efficiency, and compactness. Si-based approaches usually have slower switching speeds and increased energy loss, especially at higher frequencies. In contrast, the fast electron mobility and wide bandgap feature of GaN transistors helps to minimize switching loss, thereby helping to either minimize loss or to increase switching frequency. Higher efficiency of GaN-based inverters also means less stringent thermal management. Si-based designs rely on bulky heat sinks and cooling systems in order to dissipate the substantial heat generated by higher losses. GaN devices, by their lower loss operation, dissipate less heat which in turn simplifies cooling solutions. Not only does this simplify the system design, but it also leads to even lower size and cost reductions. In spite of the many benefits of GaN transistors, they also introduce challenges, most notably with driving and controlling these high-performance devices. Gate control for GaN transistors is often more complex than that of MOSFETs, so they require a gate driver with integrated fast switching and high voltage / gate current drive capability under high power conditions. These drivers should also prevent the GaN transistors from overvoltage and overcurrent that could result in damage to the devices. In addition, GaN transistors do achieve better performance with higher switching frequencies, but it also means you need to pay attention to the layout and design considerations like minimising parasitic inductances and thermal management.

In this chapter, we will explore the GaN-based inverter, focusing on power stage specifications and high-level partitioning.

3.1 Specifications

It is important to consider the key specifications of a GaN-based inverter as all of these specifications will ultimately dictate the performance, reliability and suitability of the Galium Nitride-based inverter for the particular application. This section describes the informed spec for a GaN inverter such as input & output voltage, power, switching frequency, efficiency, thermal management and electromagnetic interference considerations. GaN-based inverters facilitate a variety of performance advantages; however, the design process comprises of a series of critical specifications, which must be calculated to ensure that the device will achieve its target operational parameters.

Table 4: Inverter specifications

Ambient Temperature	°C	65
Nominal Voltage	V	400
Nominal Switching Frequency	Hz	20000
Maximum Switching Frequency	Hz	50000
Maximum Drain Current	A	150

In this specific case, the inverter is required to operate at a nominal voltage of 400 V with a frequency not exceeding 20 kHz. However, for a worst-case scenario analysis, the performance was evaluated at a 50 kHz switching frequency, taking into account various losses and thermal considerations. The nominal voltage of 400 V is typical for high-power inverters, particularly those used in industrial applications, renewable energy systems and electric vehicle powertrains. The inverter operates at this voltage level and, therefore, must be designed for large power outputs with efficiency and reliability.

In the context of the design, three Nexperia GAN039-650NTB in parallel for each leg have been selected to produce a drain current capacity of 150 A for each phase. The device is a normally-off transistor for high power and high frequency applications, merging high voltage GaN HEMT technology with low voltage silicon MOSFET technologies, delivering state-of-the-art performance and unmatched reliability. This polymer based transistor was selected as this makes the design very efficient and helps to minimise power losses and the overall

dimensions of the inverter. These capabilities clearly separate GaN devices as the inverter technology of the future for high power and high frequency, optimizing high-performance and energy-efficient designs.

With all of these features combined with a 650 V drain-source voltage (V_{DS}) which allows it to operate at high voltages, this device is an ideal candidate for high efficiency high voltage DC bus systems such as solar inverters or other types of industrial inverters. Maintained in high voltage at excellent performance, large voltage level is a major advantage to the high power application for this device. In addition, the low $R_{ds(on)}$ (typically 33 mΩ at 25 °C) offers minimized conduction losses. At higher temperatures like 150 °C, the resistance is still efficient at 73 mΩ. This low resistance help minimize energy lost during operation, making way for better overall system efficiency. The gate-source voltage (V_{GS}) threshold is another important parameter that describes the voltage difference between the gate and source terminals when the field-effect transistor starts to conduct, allowing current to flow. In other words, it serves as the rank that signals the changeover of device state from OFF to ON. In GaN transistors, it is generally lower than conventional silicon MOSFETs, making possible fast switching speed and low power consumption. The $V_{GS(th)}$ is around 4 V for the GAN039-NTB: a lower $V_{GS(th)}$ ensures faster ON transition of the transistor, which is beneficial for devices for high frequency applications due to faster transition. Moreover, the strong gate design with ±20 V gate-source voltage (VGS) rating is a further key component of transistor reliability, especially in electrically noisy environments. This broad V_{GS} range enables the device to withstand even sporadic, extreme over-voltage conditions without inflicting gate structure damage. This robustness is crucial to ensure stable operation in the presence of potential gate bounce, a situation that can cause undesired oscillation in the device due to rapid switching events or external electrical noise. Furthermore, the transistor's low gate charge (Q_G) of 26 nC and gate-drain charge (Q_{GD}) of just 5 nC make it ideal for fast switching transitions that minimize additional losses associated with switching. This makes it important for high frequency applications where minimal switching losses contribute to improved overall efficiency. CCPAK1212i, from its thermal component reduces hot spots and improves overall thermal performance. With a low thermal resistance, the package ensures that the device can sustain high thermal loads while still being operated at junction temperatures of up to 150 °C, a factor of paramount importance to bipolar reliability in high power applications [28].

The conduction losses in the GaN FETs are directly related to the $R_{DS(on)}$ value and the current flowing through each device. In our case the $R_{DS(on)}$ for each GaN FET is maximum 39 mΩ at 25 °C. For three devices in parallel, the effective $R_{DS(on)}$ for the combined leg is reduced, which helps to lower the overall conduction losses.

The conduction losses for each leg of the inverter can be calculated as follows [29]:

$$P_{COND} = I_D^2 \cdot R_{DS(on)} = 150^2\ A \cdot \frac{39\ m\Omega}{3} = 292.5\ W \quad (5)$$

While the inverter is designed to operate at a nominal switching frequency of 20 kHz, it is essential evaluate its performance at a worst-case switching frequency of 50 kHz. Higher switching frequencies allow for smaller passive components and reduced output filtering, but they also result in increased switching losses. Switching losses are a significant contributor to total power loss in high frequency inverters. These losses occur during the transitions between the ON and OFF states of the transistors and are directly proportional to the switching frequency.

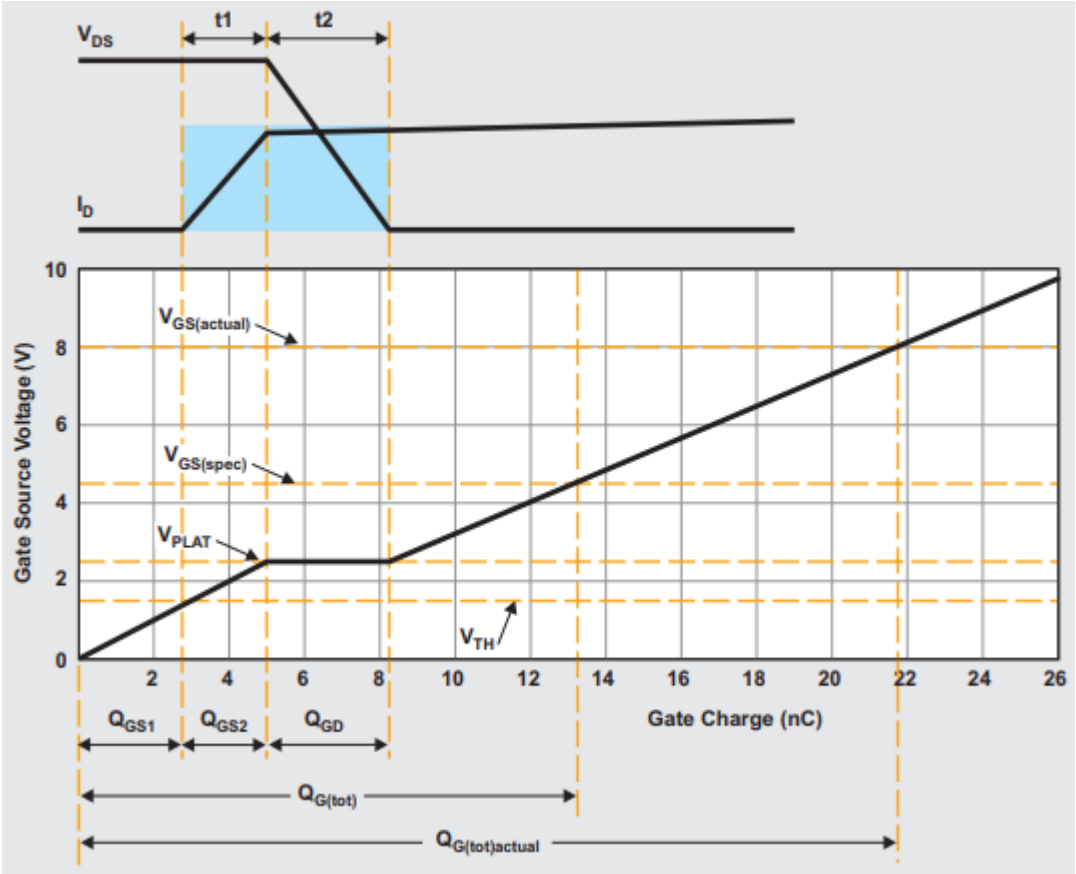


Figure 9: Switching losses [29]

The switching losses can be estimated using the formula [30]:

$$P_{SW} = \frac{1}{2} \times V_{DS} \times I_D \times (t_{on} + t_{off}) \times f_{SW} \quad (6)$$

Where, Q_{GS2} and Q_{GD} depend on the time the driver gets to charge the FET and I_G is the gate current. Taking from the datasheet the values at 25 °C with V_{DS}= 400 V, $R_{(ext)}$= 30 Ω and V_{GS}= 10 V, we get:

$$P_{SW} = 0.5 \times 400\ V \times 150\ A \times 64\ ns \times 50\ kHz = 96\ W \quad (7)$$

The total losses for each leg at 50 kHz can be estimated by adding the conduction losses and the switching losses:

$$P_{TOT} = P_{COND} + P_{SW} \quad (8)$$

3.2 High-level partitioning

High-level partitioning is an essential step in the design of any power converter, especially a GaN-based inverter, where various functional blocks are integrated to achieve optimal performance, efficiency and scalability. In this section, the inverter design has been broken down into key blocks that play distinct role in power conversion, control and protection. Dividing the design into its functional constituents simplifies the overall design and increases the level of modularity, which are both important for prototyping as well as future development..

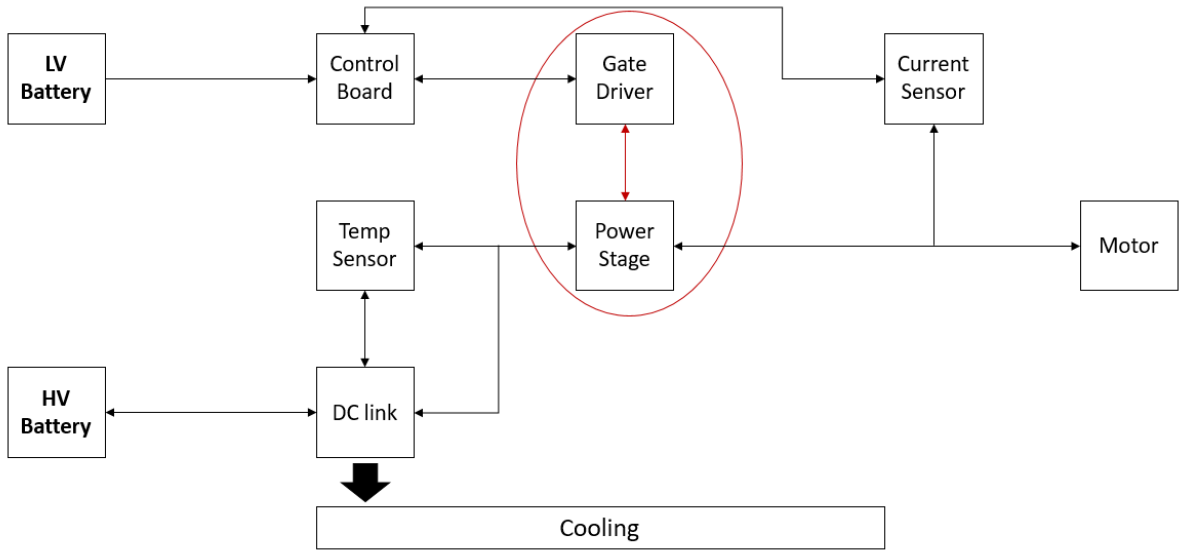


Figure 10: High-level partitioning of an inverter system

3.2.1 Power Stage

Of all sections of a GaN-based inverter system, the power stage may represent the most challenging and critical element, as it is responsible for performing the basic function of DC-AC power conversion. This process is accomplished using high-speed switching transistors, in this case GaN devices, that far exceed traditional silicon MOSFETs in efficiency, speed and power density. The choice of the power stage design has a big impact on the overall inverter performance: efficiency, form factor, and power capability.

The power stage of a GaN-based inverter can be divided into:

- GaN transistors: The main switching devices used in the power stage. These devices are wide bandgap, and can operate at higher voltages, switch faster and create less loss than silicon-based devices. As GaN has a high electron mobility, it allows very fast switching on the order of nanoseconds — over such switching times are dominant and can significantly reduce switching loss while enhancing efficiency. GaN transistors are typically arranged in a half-bridge or full-bridge configuration during the power stage. To create a complete AC waveform, a full-bridge configuration (four transistors) is preferred. Such configuration provides output positive and negative voltage from inverter which is needed for AC load. GaN devices provide operation at higher switching frequencies in these configurations, which means smaller passive components and a smaller overall footprint.
- Figure 11: Three-phase bridge GaN voltage-source inverter [31]

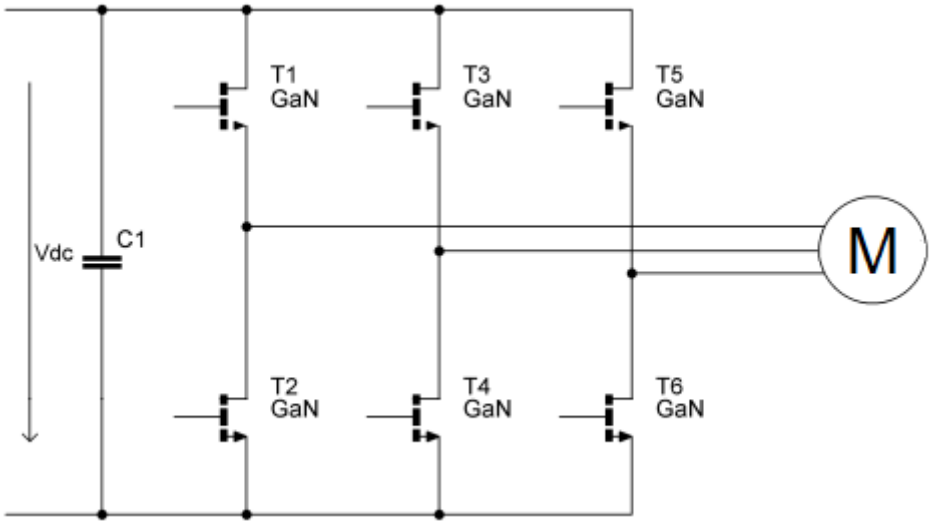


Figure 12: Three-phase bridge GaN voltage-source inverter [31]

- DC Link: the power stage usually contains DC Link, which include the energy storage required to support the GaN transistors switching action. These capacitors play a role in smoothing the input voltage and delivering a uniform DC supply to the switching elements. In order to reduce losses and guarantee a fast transient response, low-ESR capacitors are applied due to the fast switching nature of GaN transistors. The choice of capacitors in the power stage plays a direct role in both the inverter's performance under voltage spikes and its ability to manage ripple, especially important in high-frequency designs..

The performance requirements for the inverter, coupled with the application, then determine the switching topology used in the power stage. High output power is generated using full-bridge topology. The frequency of PWM is determined by the ON and OFF sequence of each transistor in the full-bridge configuration, which is controlled using the gate driver circuit to switch ON and OFF. The filtered signal generates a clean AC output waveform.

In traditional silicon-based designs, hard-switching is commonly used, where transistors are switched on and off with significant voltage and current across them, leading to high switching losses and increased thermal stress. In contrast, soft-switching techniques greatly reduce these losses by ensuring that transistors switch when the voltage or current is minimal. This is particularly advantageous in high-frequency applications, where switching losses can become a significant portion of the total power loss. Soft-switching techniques such as ZVS and ZCS could be advantageous for enhancing the efficiency of the power stage in GaN-based inverters [32].

GaN transistors are very efficient, but power stage does emit some heat during high-power operation. Thermal management is key to prevent early failures of the inverter which is critical for performance and failure analysis. Nets And FansUnder the right conditions, GaN devices generate far less heat than their silicon counterparts, so the power stage design will usually feature heat sinks and, in some instances, active cooling (fans or liquid cooling) to dissipate the heat developed by the GaN devices. Thanks to GaN transistors' higher efficiency, GaN has significantly less demanding thermal management requirements than silicon-based systems, though thermal design is still important to avoid localized hotspots and operate safely at high power levels.

3.2.2 Gate driving circuit

Gate driving circuit is an important part of the power stage of an inverter, especially if GaN transistors are used in the power stage. Fast, precise, and controlled gate signals are essential to make the most of the high-speed switching and low losses that GaN transistors can deliver. A good gate driver will make sure that the transistors are turned on and off at their optimal performance scope, reducing switching losses, protecting the transistors from damage and overall improving the efficiency of the inverter.

The gate driver circuit in a GaN-based inverter is responsible for generating the appropriate signals to control the on/off states of the GaN transistors. A typical gate driver circuit can include:

- Driver IC: The driver IC is the heart of the gate driving circuit, this chip is responsible for converting control signals from the microcontroller into high-speed gate signals — the gate signals needed for the operation of the GaN transistors. GaN transistors typically work at much lower gate voltages (usually 5V to 6V) than silicon MOSFETs, and the driver IC must be able to generate those exact gate voltages, with very fast rise and fall tones, to maximize the switching speed, while minimizing losses.
- Bootstrap Circuit: employed to generate the high-side gate voltage in many inverter designs, particularly those utilizing high-side and low-side switching configurations. This also allows the gate driver to float with respect to the source terminal of the high-side transistor, allowing it to control the high-side transistor properly when operating it in high-side mode. In the low-side conduction phase, the bootstrap capacitor is charged and then used to provide the gate voltage in the high-side switching phase.
- Level Shifters: For some designs where both high-side and low-side switching is required, use of level shifters are also very common in letting

control signals sent to the high-side transistors are properly referenced to the floating source potential. These results enable the gate driver to control the transistors accurately whether they are in high-side or low-side positions, and to do so without creating damaging voltage gain spikes or delaying the switching process.

- Power Supply for Gate Driver: Stability and low noise of the power supply is essential for the gate driver to operate. The power supply must produce the correct gate voltage with low enough ripple voltage that the gate circuits do not switch erroneously or produce noise. Isolated power supplies are used in many applications to provide separate biasing for the high-side and low-side gate drivers to ensure there will be no unwanted interaction between the control signals.

Although many of the fundamental principles of driving transistors are the same regardless of the underlying technology, GaN transistors do pose unique challenges compared to standard silicon MOSFETs. The cause of these challenges are the original electrical characteristic of GaN devices such as their the higher switching speeds, lower gate charge and their higher sensitivity to parasitic inductances and capacitances. The main challenge is that they can switch at very high speeds, with rising and falling times often measured in nanoseconds. This swift toggling enhances efficiency and minimizes losses but imposes on the gate driver circuit the requirement to produce clean and well-formed signals with minimum delay or distortions. Any signal distortion or delay can have a huge impact on switching losses or, even worse, lead to improper transistor switching, potentially causing devices to fail. GaN transistors also have a very low gate charge, so they can switch faster than their silicon MOSFET counterparts. This characteristic is a problem for the gate driver, though, because gate overdrive can cause overshoot, high-power dissipation, and gate oxide breakdown. This is why it means precision when it comes to voltages levels supplied by the gate driver so it doesn't get harmed. The requirements for the gate driver are also unique, as the gate threshold voltage of GaN transistors is lower than that of silicon devices. Gate voltage noise could also cause spurious switching events, leading to lost work and ultimately damaging the transistors. Moreover, the very high switching speed of GaN transistors increases their sensitivity to parasitic inductances and capacitances of the gate driver circuit. RF signal degradation, ringing, overshoot, and turn-off delay can occur from parasitic elements, particularly inductance from the gate loop, resulting in high-frequency oscillations that can damage the FET transistors in high power applications. Common-mode currents can couple through traces on a PCB that act as antennas and properly layout the PCB to keep trace lengths short and use low-inductance components. However, because GaN transistors are high performance and fast-switching transistors, protection mechanisms are an important requirement in the gate driver circuit to avoid

failures and guarantee long-term stability. Overvoltage protection: Transient over-voltages can lead to destructive breakdown of the gate oxide and thus it is necessary to protect the gate voltage such that it does not excess a safe value. The desaturation detector observes the voltage across the transistor and turns off the driver should an unusually high voltage be detected in order to indicate a possible short-circuit condition. Miller clamping also stabilizes the gate voltage during fast-train switching, preventing parasitic switching due to capacitance between gate and drain. Finally, dead time control is integral to prevention of shoot-through in inverter designs, where both high-side and low-side transistors can turn on simultaneously and cause catastrophic failures. Accurate dead time management ensures that the transistors are protected while minimizing conduction losses, thus optimizing the efficiency of the inverter system [33].

3.2.3 Control system

A GaN based inverter controller is a vital element of this technology, as it directly impacts how well the inverter will function as a whole by providing power stage control and regulating switching signals and stability at different load conditions. It employs a closed-loop control system that detects changes and adapts to them, maintaining voltage and frequency regulation. The control system is also responsible for implementing protection mechanisms and responding to fault conditions, making it an essential element for the inverter's reliability and performance. The control system of an inverter typically consists of the following parts:

- Microcontroller/Digital Signal Processor (DSP): the control system consists of a microcontroller or DSP, which implements the control algorithms, generates the switching signals and reads feedback from sensors. When controlling GaN transistors (which enable fast switching), we need to make sure that any embedded control systems can cope with quick dynamic behaviors. Such real-time processing of high-frequency, complex control algorithms, like PWM, makes a DSP preferable in many applications.
- PWM Generation: One of the main methods that can be used for controlling switching of GaN transistors integrated in the power stage of a system is pulse-width modulation. The control system changes the output voltage of the inverter by modulating the duty cycle of the PWM signal. With their high-frequency switchability, GaN transistors make higher-resolution PWM possible — leading to finer steps in output waveform control. These enable the control system to create a PWM signal with precise transitions to increase efficiency and minimize distortions.

- Feedback Loops: the control system focuses on feedback from voltage, current, and temperature sensors for stable operation. The controller receives this real-time data from the sensors and adjusts the PWM signals as needed. The feedback loops allow the system to adjust dynamically to variations in load conditions or changes in input voltage, keeping performance within specified limits. One such application is a voltage controller where during load condition voltage drops so control system increases duty cycle applied to PWM signal.
- Control Algorithms: There are many control algorithms that can be utilized in the control system for managing the inverter's performance. PID (proportional-integral-derivative) control is the most widely implemented control technique which modifies the output based on the difference (error) between the desired and the actual output values. PID control is simple but works well for a majority of applications. Nevertheless, advanced control methods, including model predictive control (MPC) and sliding mode control (SMC) have been developed and are being applied to GaN inverters with high efficiency. This enables improved dynamic performance compared to simpler strategies, and can better accommodate nonlinearities in the system.

GaN-based inverters utilize control strategies that allow for optimal utilization of GaN transistor's fast-switching features with reduced losses and stable operation. The two well known control strategies include voltage-oriented control (VOC) and current-oriented control (COC).

VOC is an extensively employed mechanism for PBS output voltage conversion of inverters like renewable sources and UPS. In VOC, the control system directly controls the PWM signals to keep the output voltage stable regardless of input voltage and load variations. With a feedback loop monitoring the output voltage, the PWM duty cycle is adjusted as necessary so as to minimize the difference between the output voltage and the target value. Based on its main function of output current controlling of the inverter, COC is the most widely used one in such applications requiring accurate control of the output current, most scientific of them include motor drives or gird tied inverters. In COC, the control system tracks the output current and corrects the switching signals so that the current follows the reference value. However, this method allows more precise control over the power provided to the load, making it optimal for uses with dynamic load conditions [34].

3.2.4 Sensors

In Control Techniques' high performing mid-range in-vehicle current, temperature and pressure sensors are critical for GaN-based inverters to enable optimal performance and protect components of system. These sensors send signals to the control system in real-time, which uses the information to maintain power flow, prevent overloading, and avoid overheating. This information enables the inverter to dynamically adjust its operational parameters to optimise performance under varying load conditions. The total current measurement is important for controlling the power delivered, and it also provides a protection mechanism, such as overcurrent shutdown and short-circuit detection. A frequent way to measure current is with a shunt resistor. Small resistors are added in the current path and the voltage drop across those is read to know the current. Shunt resistors ensure accuracy and speed of response, parameters of great importance in a fast-switching environment like that of GaN transistors. They do produce heat that needs to be managed, especially in high-power applications. Hall-effect sensors are another common method for current sensing providing electrical isolation with the ability to measure AC and DC currents. A Hall-effect sensor is non-intrusive and adds safety by electrically isolating the measurement circuitry from the high-power components. Current transformers are often used in applications to measure high AC currents providing isolation and low power dissipation but not suitable for measures in DC current. The high-speed switching characteristics of GaN transistors make the current sensing issue in GaN inverters particularly difficult. Indeed, fast switching leads to fast changing current which is why we need sensors that suit low response time and allow us fully release those delays. The second point is that the sensors need to bear the high power levels that are characteristic of this type of inverter without saturating or heating. The output of these sensors need to be filtered for noise, and properly calibrated, as an erroneous measurement could affect the inverter performance and safety. Temperature sensing is just as important, as the high power of inverters can lead to thermal stress. GaN transistors are more sensitive to temperature extremes than traditional silicon devices, and failing to manage temperature extremes can degrade their performance, even cause failure. In comparison, stable and low-cost temperature measurement systems are usually made using thermistors, which also show high sensitivity. Negative temperature coefficient (NTC) thermistors are often used to measure the temperature of heat sinks or power devices. Thermistors, on the other hand, require calibration and can be complicated to use because the resistance is non-linear with respect to temperature. Alternatively, resistance temperature detectors (RTDs) are a more accurate and stable option, but are often more costly and may not always be necessary depending on the application. In some scenarios, GaN transistors or gate drivers may already have embedded temperature sensors, enabling direct junction temperature measurements. These combined sensors enable real-time assessment of the

device's temperature, so the control system can modulate or shut down the inverter if overheating occurs. The biggest obstacle for temperature sensing used in GaN inverters is the correct and real-time sensing of temperature variations during high-power operations where the temperature may accelerate abruptly. All the sensors need to be placed suitably near components that generate heat, and the control system needs to be able to respond quickly enough to bursts of temperature to prevent thermal damage. In such mission-critical, high-performance systems, having a sound thermal management strategy in place is essential, which goes hand in hand with how you choose a suitable sensor and ensure it's operational in the inverter's fast-moving environment. In summary, both current and temperature sensors are essential to monitor the operation of GaN-based inverters, ensuring high system performance and long-term reliability. Measurement with accuracy and timeliness perform with dynamic adjustment for system operation, ensuring safe and efficient power conversion. Through this study, by using correct sensors with careful decision, low the high power high speed switching activities risk inductor inverter design to increase risk and reliability.

Chapter 4

Design of a GaN-based inverter power stage

The most important subsystem responsible for an inverter design is its power stage that encompasses several key components, which should cooperate in such a way to ensure that the conversion of dc power into ac power will be carried out effectively, confidently and by taking care with the safety issues.

This paper is methodically divided into sections scrutinizing each element that contributes to the successful shaping of the inverter system from switching frequency and efficiency to thermal management and EMI considerations & converter topology to address the technical challenges associated with their performance. This need for higher efficiency, lower losses, and room for more compact designs has driven the implementation of advanced semiconductor materials and topologies in inverter power stages. For successful implementation of these systems, the inverter must maintain the power quality, minimize the harmonic distortion, and ensure reliable operation under changing load conditions.

In this chapter, we will discuss the design and implementation of the inverter power stage, including the common components that form the overall system. The implemented design will be discussed in detail, together with relevant topics, like converter topology, gate driving circuit, power supply and sensors. Also, the layout considerations, important to minimize parasitic effects and maximize the thermal management, will be presented.

4.1 Schematic

4.1.1 3-phase bridge

The 3-phase bridge topology is one of the main topologies for power conversion applications, such as drives, converters, inverters, and industrial equipment, where high power conversion capability is critical. It basically is a combination

of 6 switching elements, where for every phase you have one pair of switches: a high-side and a low-side switch. These switches successively connect each output phase to the positive (or negative) side of the DC bus according to a modulation strategy, often pulse-width modulation (PWM) based in order to create a sinusoidal function at the output across the load.

In this topology:

- Three legs are refers to the three phase of inverter output (A, B and C).
- There are two switches (high-side and low-side) in series connected to the DC bus for each leg.
- Each leg of the inverter will contain the midway point for which each phase is output.

The primary operation of the 3-phase bridge is to transform a DC input voltage into a 3-phase AC output, which is required for driving AC motors or interfacing with 3-phase power networks. Using transistors as the switches enables fast switching of ON and OFF states, thus allowing accurate output waveform control and giving benefits like high efficiency, high power handling ability and high reliability.

There are several benefits of this topology, that make it a goto topology for most high power derived applications. Here are a few of the major advantages:

- High efficiency: one of its most practical advantages is its ability to produce balanced 3-phase AC power instead of the switching losses typical of the inverter. It introduces greater overall efficiency, which is especially beneficial in applications such as electric vehicles and renewable energy systems in which energy efficiency is critical.
- Harmonics reduction: the symmetric structure of the 3-phase bridge leads to less harmonic distortion generation Harmonics are not desired because it leads to more losses and heating and therefore reduces the systems efficiency through motors, etc. This results in a smoother sinusoidal output waveform, which is better for the performance and longevity of the motor, as well as for any connected loads.
- Power is distributed evenly: in a 3-phase system, the power is delivered more uniformly across three phases, allowing the electrical load to be balanced. This balance: provides smoother operation, less stress on components, and more reliability over time.
- Compact design: 3 phase bridge topology allows compact inverter design This means the inverter can still drive high power while minimising the overall device weight and system size, perfect for space and weight critical applications [35].

As the required current to this design is quite high (150 A), using a single GAN039 would be impossible due to it's low current capacity. Achieving the 150 A current required by our system took a different direction. The current specification is high and thus parallelization technique is used to meet this. Parallelization of transistors : (a very common technique in high energy applications. This allows current to be distributed over multiple devices thus reducing stress on specific components, increase system reliability.) This is especially useful in a three phase inverter casing where it enables the inverter to process high currents while reducing the thermal loads on each transistor.

This methodology provides many advantages, especially in cases of high power density and efficiency requirements:

- Improved current handling: parallelization increases the overall current capacity available in each individual phase without stressing out any particular transistor, which means that the inverter is capable of handling more load and doing so within its safe operating area of operation.
- Less conduction loss: conduction losses in a transistor are proportional to the ON-resistance and the conduction current. The additional benefit of using the switch in parallel is that when splitting the current between multiple transistors, each individual device is able to conduct a lower amount of current, therefore reducing conduction losses and increasing efficiency.
- Enhanced thermal performance: thermal management is one particular challenge in power electronics; when using transistors, some of the input energy will always generate heat. In addition, thermal load can be shared by multiple devices by means of the parallelization method which decreases the transistors temperature rise and risk of thermal runaway [36].

Dynamic power consumption from transistors poses challenges in driving inverters, especially if the inverter drive is parquetized to withstand more current. The dynamic power is the power consumed in a transistor switching event, where the gate capacitance will charge and discharge for each cycle. In high-frequency applications, where energy must be supplied to transfer charge through the gate capacitance during each switching cycle, this power becomes much important. As with all transistors, C_{iss} adds in parallel when we parallel transistors, so the total capacitance is multiplied. The higher capacitance means that the gate requires more power to switch effectively, which in turn affects the design of the gate driver circuit and power supply

For each switching cycle, the dynamic power needed to charge and discharge the total gate capacitance is given by:

$$P_{dyn} = \frac{1}{2} \times C_{iss(tot)} \times f_{SW} \times V_{GS}^2 \quad (9)$$

Where $C_{iss(tot)}$ is the total input capacitance of the parallelized transistors, f_{SW} is the switching frequency and V_{GS} is the gate-source voltage, which in this case is chosen at 12 V.

Given that three transistors GAN039-650NTB in parallel have been used, each with individual input capacitance of approximately 2 nF, the total input capacitance is:

$$\mathrm{C_{iss(tot)}} = 3 \times 2\ \mathrm{nF} = 6\ \mathrm{nF} \quad (10)$$

At a switching frequency of 50 kHz (worst-case), the total dynamic power needed to drive the gates of three parallelized GAN039-NTB650 is calculated as follows:

$$\mathrm{P_{dyn}} = \frac{1}{2} \times 6\ \mathrm{nF} \times 50\ \mathrm{kHz} \times 12^2\ \mathrm{V} = 21.6\ \mathrm{mW} \quad (11)$$

Therefore, the total power needed to drive six switches is:

$$\mathrm{P_{dyn(tot)}} = 6 \times 21.6\ \mathrm{mW} = 129.6\ \mathrm{mW} \quad (12)$$

After determining the dynamic power, the next step is to get the current that will flow through the gate of each transistor. This gate current requirements directly impacts gate driver selection and power supply design since the driver must be capable of supplying this current continuously, up to the specified switching frequency. The gate current can be derived from re-ordering the dynamic power formula, but in this instance we add the external resistor $R_{G(ext)}$. Gate resistors are important, as they control the rate of switching transients and the current through each transistor greater. The RMS current through the gate circuit, which represents the effective current that the gate driver must supply, is calculated as:

$$\mathrm{I_{G(RMS)}} = \sqrt{\frac{\mathrm{P_{dyn}}}{\mathrm{R_{G(ext)}}}} \quad (13)$$

It becomes clear that, in the process of selecting the appropriate gate resistor, choosing a higher resistance value results in lower current. By increasing the gate resistance, we will have a decrease in the current drawn by the gate, which affects the overall power dissipation and the switching speed. Therefore, selecting a higher resistor value provides better control over currents but it makes the system slower.

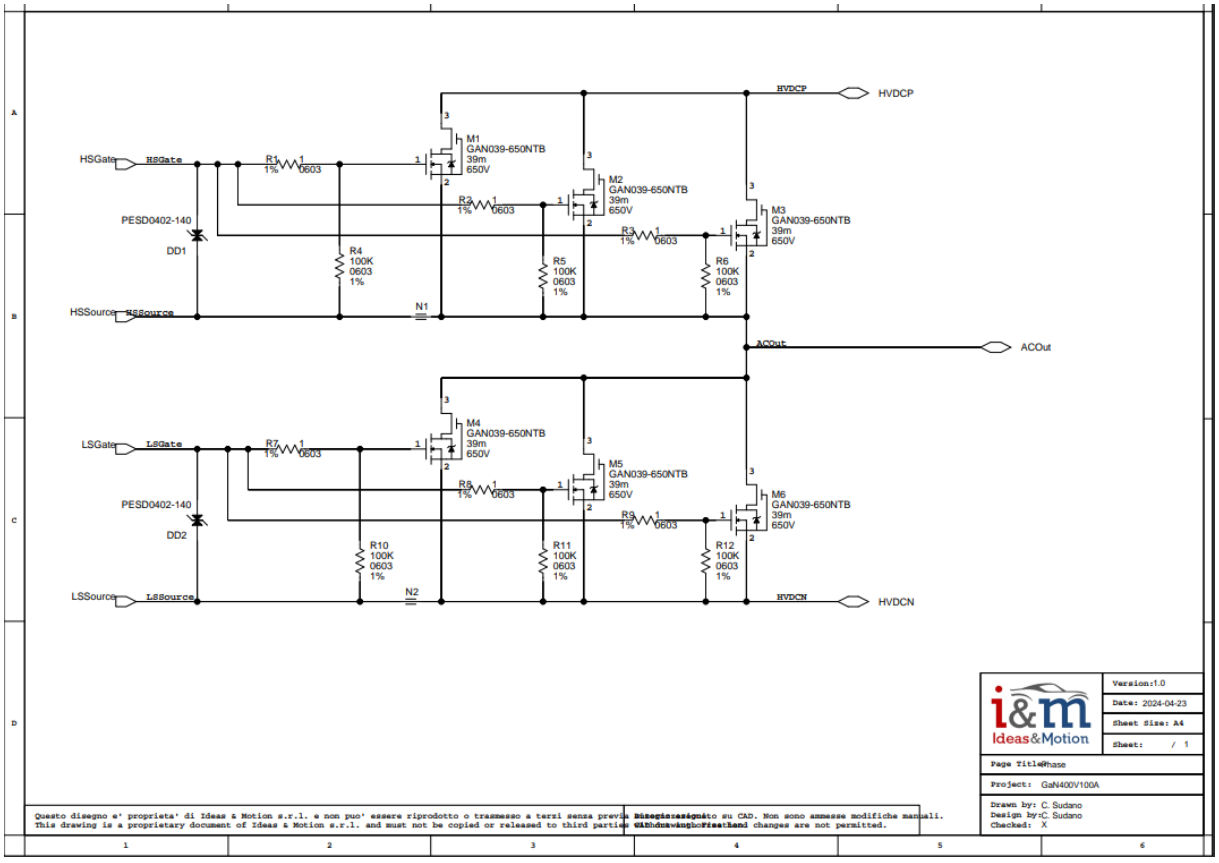


Figure 13: schematic of an inverter leg with three parallel GaN HEMTs

4.1.2 Gate driving circuit

As previously mentioned, Gallium Nitride transistors are known for their high switching speeds, high electron mobility and better thermal efficiency compared to silicon-based devices. However, the very advantages that make GaN transistors ideal for high performance applications also introduce specific challenges in gate driving design. These transistors require precise and optimized gate driving circuits to ensure efficient switching, prevent failures and minimizing energy losses. Unlike traditional silicon MOSFETs, GaN transistors typically have much lower charge, faster switching times and higher voltage handling capabilities.

Consequently, a careful gate driving strategy is crucial to fully exploit their potential while mitigating parasitic effects like ringing and overshoot, which can lead to device failure if left unchecked.

This section discusses the essential aspects of designing the gate driver circuit for GaN-based 3-phase inverters, with specific focus on the implementation of the 2EDR6258X driver. We will examine its key technical features, such as galvanic isolation and high frequency driving capabilities, which make it particularly well-suited to address the challenges posed by GaN devices.

The Infineon 2EDR6258X is a dual-channel isolated gate driver designed for driving both SiC MOSFETs and GaN HEMTs power switches. It offers a variety of features that make it highly suitable for high efficiency and high speed switching applications, such as power supplies, electric vehicle chargers and industrial converters. Here is a detailed overview of its main characteristics:

- Dual-channel isolated gate driver: it supports two independent output channels (OUTA and OUTB), which allows it to drive two separate switches simultaneously.
- Fast switching and low propagation delay: the driver has an input-to-output propagation delay of just 38 ns with excellent stability (+9/-5 ns), enabling fast switching, which is essential in high frequency application like GaN-based inverters.
- High current capability: the driver can source 5 A and sink 9 A, which is critical for driving GaN HEMTs with low gate resistance and ensuring fast switching transition.
- Wide operating voltage range: the input-side supply voltage (VDDI) ranges from 3 V to 17 V, making it flexible for different application requirements. The output-side supply voltage (VDDA and VDDB) operates up to 20 V.
- Undervoltage lockout (UVLO): both the input and output sides are protected by UVLO. This prevents damage to the power switches by ensuring they do not turn ON when the supply voltage is below a safe threshold.
- Soot-through protection and configurable dead-time control: it includes an STP/DTC pin that prevents soot-through, a condition where both high-side and low-side switches are ON simultaneously. Dead-time can be configured via an external resistor.
- Reinforced isolation: the driver uses coreless transformer technology to provide isolation between the input and the output sides, ensuring high common-mode transient immunity (CMTI) of over 150 V/ns. This is

particularly important in noisy environments where switching transients could affect signal integrity [37].

In our design, three 2EDR6258X gate drivers were selected, with one driver dedicated to each leg of the inverter. This choice allows precise and independent control over each leg, optimizing switching performance and ensuring stable operation across the inverter's phases. Using separate drivers enhances the system's flexibility in managing each leg's specific current and voltage requirements, improving both efficiency and thermal performance.

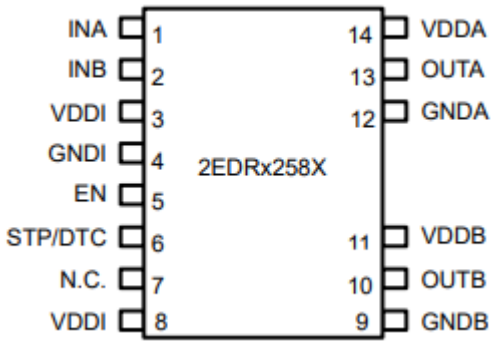


Figure 14: Pin configuration [26]

In the design, each driver is carefully configured with specific connection and components to ensure optimal performance for each leg of the inverter. Below is an overview of the main pins and the choices made for each in this design:

- VDDI (Input Side Supply Voltage): this pin is connected to a stable and low-noise power source (typically 5 V**)** to power the input circuitry of the driver. A minimum bypass capacitance of 100 nF was added, as recommended in the datasheet.
- VDDA and VDDB (Output Side Supply Voltages**)**: these pins supply power to the high and low output stages, respectively to a 12 V isolated source. This voltage provides adequate drive strength for the gates, ensuring they can be fully switched ON and OFF for fast and efficient transitions. Bypass capacitors of 100 nF are placed close to each VDDA and VDDB pin to stabilize these supplies and filter out any ripple or noise that could affect performance.
- GNDI and GNDA/GNDB (Ground Pins): GNDI is connected to the ground on the input side. GNDA/GNDB is connected to the source of HS and LS respectively.

- INA and INB (Logic Input Signals): these pins receive control signals from the PWM controller, allowing the driver to respond to high and low commands for switching the GaN FETs.
- OUTA and OUTB (High and Low Side Outputs): these outputs pins drive the gates of the GaN FETs in each leg of the inverter. The gate drive signal strength is set by configuring external gate resistors for each transistors, which control the speed of switching and help manage power dissipation. By selecting appropriate values for these resistors, we balance switching speed with thermal stability, ensuring reliable performance in high-frequency operation.
- ENABLE: this pin serves as a control input that allows the driver to be activated or deactivated as required by the system. When the ENABLE pin is high, the driver is active, allowing the output channels to respond to the control signal on INA and INB. When pulled low, the driver is disabled, effectively shutting down the output stages and preventing switching.
- STP/DTC (Soot-Through Protection / Dead-Time Control): this pin is used to set the dead time between high and low side switching, preventing shoot-through conditions that could damage the GaN FETs. An external resistor is connected to this pin, allowing us to precisely configure the dead time for each leg based on switching speed and load requirements. In the design is selected a 30 kΩ resistor which allows for a dead time of 300 ns.
- NC (No Connect): some pins on the driver may be labelled as NC, meaning they are not connected to internal circuitry. In the design, these pins are left unconnected [37].

As previously stated, in designing an effective gate driver, a crucial parameter to consider is the gate resistance. For the design, has been chosen a configuration where the turn-on (source) and the turn-off (sink) paths are separated to optimize control over each phase of switching. This setup allows us to fine-tune the switching speed by adjusting the resistance independently for the charging and discharging of the gate. Therefore, in our configuration, we have selected two 4.7 Ω gate resistors in parallel, with one resistor having an NRVBSS14 diode in series. This approach enables us to use different effective resistances depending on the direction of current flow:

- **Charging phase**: during the turn-on phase, the diode is reverse-biased, which blocks its parallel resistor path. As a result, the current flows only through the primary 4.7 Ω resistor, making the effective resistance for turn-on at that value. The current that flow through the gate in this phase is:

$$I_{G(RMS)} = \sqrt{\frac{P_{dyn}}{R_{G(ext)}}} = \sqrt{\frac{21.6\ mW}{4.7\ \Omega}} = 67.8\ mA \quad (14)$$

- **Discharging phase**: during the turn-off phase, the diode is forward-biased, allowing current to flow through both resistor in parallel. The effective resistance for turn-off becomes the parallel combination of the two gate resistances, which is simply their value divided by 2. The current that flow through the gate in this phase is:

$$I_{G(RMS)} = \sqrt{\frac{P_{dyn}}{R_{G(ext)}}} = \sqrt{\frac{21.6\ mW}{2.35\ \Omega}} = 95.8\ mA \quad (15)$$

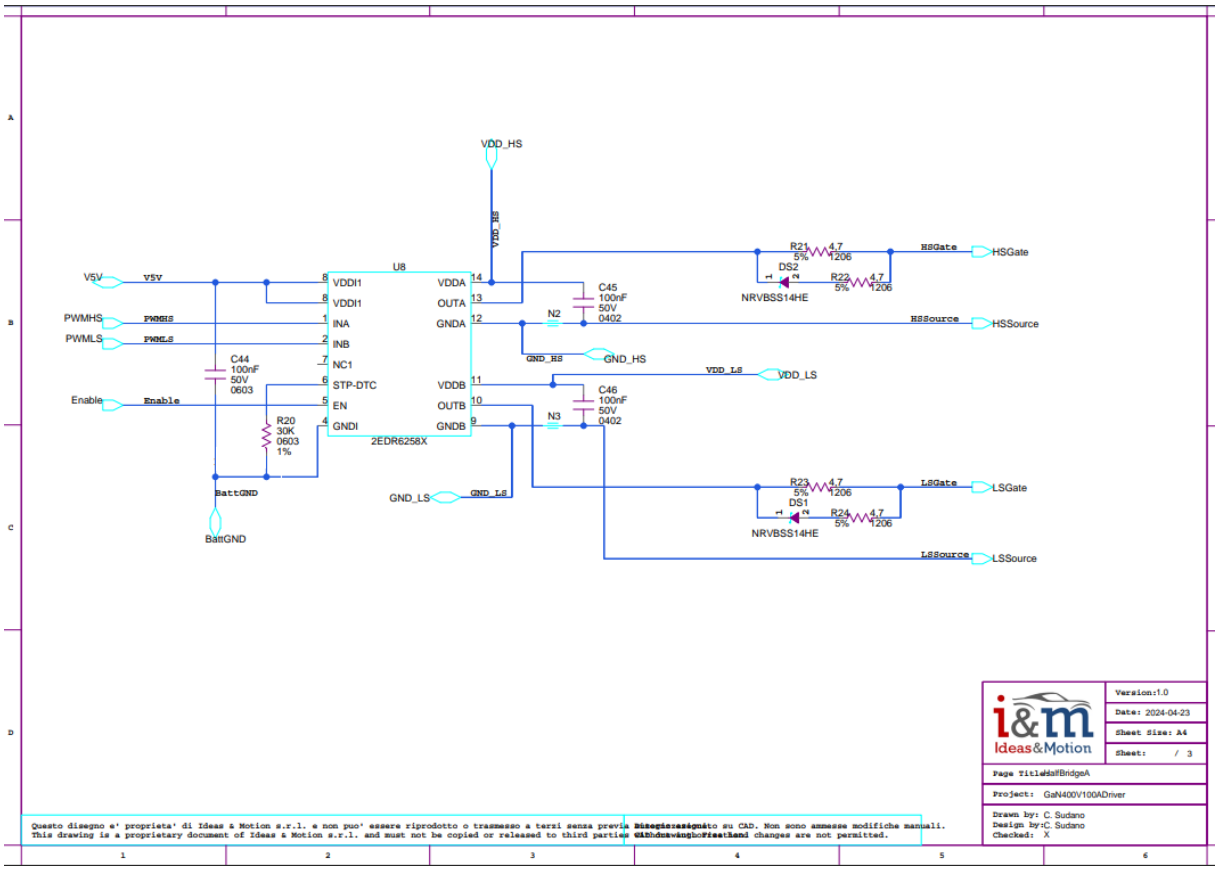


Figure 15: Schematic of the gate driver circuit

4.1.3 Power supply

In designing a GaN-based Inverter, the power supply architecture plays a crucial role in ensuring stability, efficiency and reliability. Each component within the inverter demands a specific voltage level, and in some cases, isolation from other parts of the circuit to avoid interference and maintain system integrity. Given the complex requirements of a GaN inverter operating at high-voltages, the design includes a combination of isolated converters and a non-isolated converter to create stable isolated power rails for both high-side and low-side gate drivers as well as the isolated and non-isolated sections of the monitoring and control circuitry.

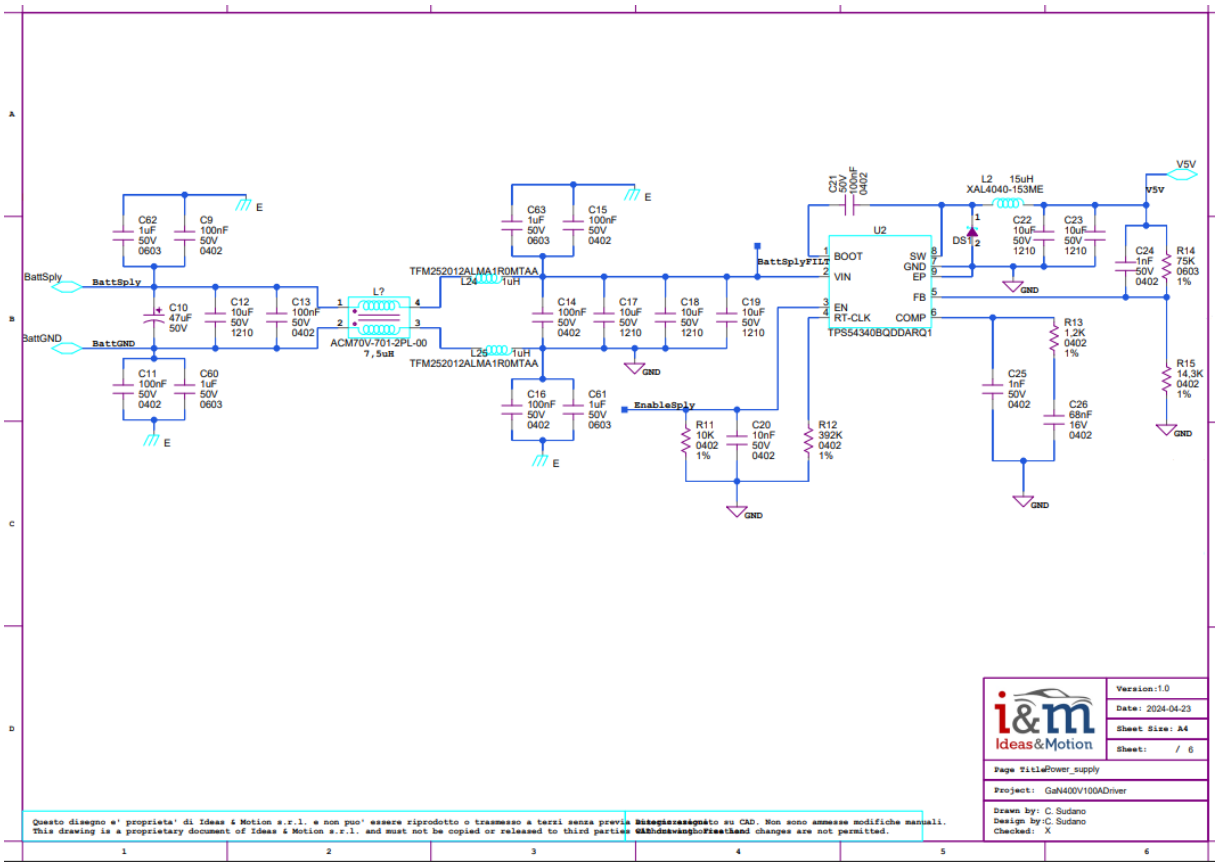


Figure 16: Schematic of the 5 V non-isolated power supply

To power the low-voltage electronics in the non-isolated sections of the system, the voltage is drawn directly from the battery and passed through a filtering stage that includes an ACM70V-701-2PL-00 common-mode choke and a set of capacitors. The choke plays a critical role in suppressing EMI (Electromagnetic Interference) by attenuating high-frequency noise, while the capacitors provide additional filtering and stabilization of the input voltage. The filtered and

stabilized voltage is then fed into a TPS54340 buck converter, which steps it down to a regulated 5 V. This ensures a clean, stable and interference-free power supply for the low voltage circuitry, critical for its reliable operation. The output of the buck is determined by a voltage divider, calculating using the following formula provided in the datasheet [38]:

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} \tag{16}$$

In an inverter application, furthermore, galvanic isolation is required to separate the low voltage domain from the high voltage domain. Using a galvanic isolation component, isolated power supplies can ensure that no current passes form the input to the output side. For DC/DC converters, a transformer provides isolation: this adds cost, increasing design complexity and reduces efficiency compared to the non-insulated counterpart.

A push-pull DC/DC converter is a transformer-isolated converter based on the buck topology, it is widely used in power electronics for isolated DC-DC conversion, particularly where efficient energy transfer and compact design are required. It operates by alternately driving two switches, which create an AC-like waveform in the primary winding of the transformer. This approach is effective in achieving isolated and stable output voltages while minimizing core losses in the transformer. Several factors contributed to the decision to use a push-pull topology for the design:

- High power density: push-pull converters provide high power density due to efficient transformer usage and symmetrical switching, which allows for smaller core sizes.
- Isolation: the topology naturally lends itself to isolation, which is critical in inverter designs where different circuit section need to operate independently.
- Efficiency: by utilizing the transformer core more effectively, the push-pull topology minimizes power losses, making it suitable for applications requiring sustained power delivery
- Voltage Scaling Flexibility: with appropriate winding ratios and configurations, the push-pull transformer can generate different output voltages.
- Reduced EMI: the symmetrical design and alternating nature of the push-pull topology tend to reduce electromagnetic interference, a key factor in this type of application [39].

To ensure proper operation of the six gate-driving circuits in the system, it is essential to supply at least four distinct reference voltages. These include one reference voltage for the low-side driver and three separate reference voltages for the high-side drivers. This requirement arises because the low-side switches share a common potential, while the high-side switches are referenced to different potentials due to their placement in the circuit topology. Furthermore, a push-pull's output is also stepped down to 5 V to generate a specific isolated voltage required to power the voltage monitor's isolator. This design choice not only enables precise and efficient gate control but also ensures compliance with the stringent requirements for galvanic isolation and reference separation in high-performance applications.

The SN6505D-Q1 transformer driver from Texas Instrument is a robust solution for driving transformers in isolated DC-DC applications. It features several design aspects that make it ideal for our application:

- Push-pull driver: designed specifically for driving transformers in isolated power supplies using a push-pull topology, ideal for compact and efficient DC/DC conversion
- Low-Noise operation: the SN6505D-Q1 is designed to minimize EMI through its push-pull switching mechanism and slew-rate control, which reduces high-frequency noise, making ideal for applications with strict EMI requirements.
- Automotive Qualified (AEC-Q100): this device is Grade 1 qualified for automotive applications, with a wide operating range of -40 °C to +125 °C.
- Thermal Shutdown Protection: this device includes thermal protection, which sluts down the driver if the temperature exceeds safe levels, adding reliability in demanding application [40].

Table 5: Power supply specifications

DESIGN PARAMETER	VALUE
Input voltage range	5 V ± 3%
Output voltage range	12 V
Maximum load current	300 mA (worst case)

This design addresses the need to convert a 5 V input to a 12 V output, providing the necessary isolated voltage for the gate drivers. The maximum current output requirement is based on the sink current needed by each driver during operation.

Given that the low-side power supply will drive three separate gate drivers, the total current capacity must be sufficient to handle three times the sink current of a single driver. This approach ensures that the design can meet the cumulative demand, maintaining stable performance across all drivers.

Direct conversion to 12 V from 5 V would typically require high turns ratio, resulting in large and potentially inefficient transformers. To optimize efficiency and stabilize the output, a voltage-quadrupling configuration is employed. In this approach, the secondary voltage of the transformer is quadrupled and then regulated down to a precise 12 V using a Low Dropout Regulator (LDO). This configuration effectively meets both the voltage and stability requirements while minimizing component size and losses. In the quadrupling configuration, each transformer output cycle charges and discharges a series of capacitors and diodes arranged to create a voltage multiplier effect.

The MIC2920A-12 fixed-voltage linear regulator by Micrel is a precise and efficient component, ideally suited to stabilize the 12 V output required in the final stage of this push-pull converter design. By selecting fixed-output regulator like this, the design benefits from simplicity, as the 12 V output does not require external resistors dividers or feedback mechanism. Positioned immediately after the quadrupling rectifier circuit, this LDO ensures a reliable and clean output voltage that supports the sensitive components downstream. A defining feature of the MIC2920A-12 is its low dropout voltage, approximately 0.5 V; this low dropout enables the regulator to maintain a steady 12 V output as long as the input voltage remains at least 12.5 V. The device's current handling capability is also suitable for our application, providing up to 400 mA of output current [41].

A rectifier diode should always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the SN6505D-Q1 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter design. The MBRS140T3G Schottky diode by Onsemi is well-suited for this application, providing a 40 V peak reverse voltage rating and a low forward current capacity of up to 1 A, both of which align with the low-power requirements of this converter. This diode has a low forward voltage drop, which is maximum 0.6 V at 1 A forward current [42].

In designing the transformer for a push-pull converter using, it is essential to carefully consider the core magnetization and turn ratios, both of which are crucial to preventing core saturation and achieving stable operation at the desired output voltage. The SN6505D-Q1 datasheet provides specific guidelines for calculating the transformer's core volt-second (V-t) product and establishing the minimum turn ratio to ensure reliable performance.

In a push-pull topology, the alternates current through each half of the transformer primary, producing a magnetic flux that oscillates across the core. The flux density (B) change in the core is proportional to the product of the primary voltage (V_P) and the time is applied (t_{ON}). The V-t product, or volt-seconds, determines the core's magnetization level per switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of B-H curve. If balanced is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region. To prevent core saturation, the selected transformer's minimum V-t product should exceed the maximum V-t product applied by the device. The maximum voltage delivered by the device is the nominal converter input plus 10%. The maximum time this voltage is applied to primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through [40]:

$$V_{t_{min}} \geq V_{IN_{max}} \times \frac{T_{max}}{2} = \frac{V_{IN_{max}}}{2 \times f_{min}} \tag{17}$$

Taking from the datasheet the f_{min} value of 363 kHz with a 5 V supply, last equation yields to the minimum V-t product for SN6505D-Q1 [29]:

$$V_{t_{min}} \geq \frac{5.5\ V}{2 \times 363\ kHz} = 7.6\ V\mu s \tag{18}$$

To determine which transformer can be driven by the device, other important factors such as isolation voltage, transformer wattage and turns ratio must be considered before making the final decision. The datasheet suggests a precise method for calculating the turns ratio; it is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typically efficiency of 97 % into account [40]:

$$n_{min} = 1.031 \times \frac{V_{S_{min}}}{V_{p_{min}}} \tag{19}$$

To achieve a stable 12 V output after the quadrupling stage, the secondary voltage of the transformer must initially 4 times lower than the value we want after rectification and regulation. By setting the secondary voltage target to a quarter of the desired output voltage, this factor allows the turns ratio to be correctly scaled to achieve the required output after quadrupling. The minimum secondary voltage (V_{Smin}) must be large enough also to account for the maximum voltage

drop across the rectifier diode (V_{Fmax}) and across the LDO (V_{DOmax}), while also ensuring the regulator input remains within its operational range. Therefore, we can determine V_{Smin} using the following equation [40]:

$$V_{S_{min}} = \frac{1}{4}(V_{F_{max}} + V_{DO_{max}} + V_{OUT_{max}}) \quad (20)$$

Then to determine the available minimum primary voltage (V_{Pmin}), the maximum possible drain-source voltage of the device (V_{DSmax}) is subtracted from the minimum converter input voltage (V_{INmin}) [40]:

$$V_{p_{min}} = V_{IN_{min}} - V_{DS_{max}} \quad (21)$$

V_{DSmax} is the product of the maximum $R_{DS(ON)}$ and I_D values for a given supply specified in the data sheet, so Equation 21 became:

$$V_{p_{min}} = V_{IN_{min}} - R_{DS_{max}} \times I_{D_{max}} \quad (22)$$

Then inserting Equation 20 and Equation 22 into Equation 19 provides the minimum turns ratio with:

$$n_{min} = 1.031 \times \frac{V_{F_{max}} + V_{DO_{max}} + V_{OUT_{max}}}{4(V_{IN_{min}} - R_{DS_{max}} \times I_{D_{max}})} \quad (23)$$

For a 5 V_{IN} to 12 V_{OUT} converter using rectifier diodes MBRS140T3G and the MIC2920A-12 Linear regulator, the data sheet values are: V_{Fmax} = 0.6 V, V_{DOmax} = 0.5 V and V_{OUTmax} = 12.5 V [41], [42].

Then assuming that the converter input voltage is taken from a 5 V controller supply with a maximum ±3 % accuracy makes V_{INmax} = 4.85 V. Finally the maximum value for drain-source resistance and drain current are taken from the SN6505D-Q1 datasheet with R_{DSmax} = 0.25 Ω and I_{Dmax} = 1 A.

Inserting the value above into Equation 23 yields a minimum turn ratio of:

$$n_{min} = 1.031 \times \frac{0.6\ V + 0.5\ V + 12.5\ V}{4(4.85\ V - 0.25\ \Omega \times 1\ A)} = 0.762 \quad (24)$$

After a thorough evaluation of the requirements and characteristics of our push – pull converter design, we selected the 760390014 transformer from Würth Elektronik. This choice was driven by the transformer's compatibility with the SN6505's operational specifications and the ability to meet the necessary volt-second product for reliable core magnetization without reaching saturation under the operating conditions. It is specifically design for push-pull applications and offers a turn ratios of **1:1.3**; for this design, the transformer was strategically inverted to achieve an effective turn ratio of approximately **1:0.77**. This inversion allows for a reduction of the turn ratio, keeping it above the calculated minimum requirement, thus preventing the secondary voltage from reaching excessive levels that would complicate regulation.

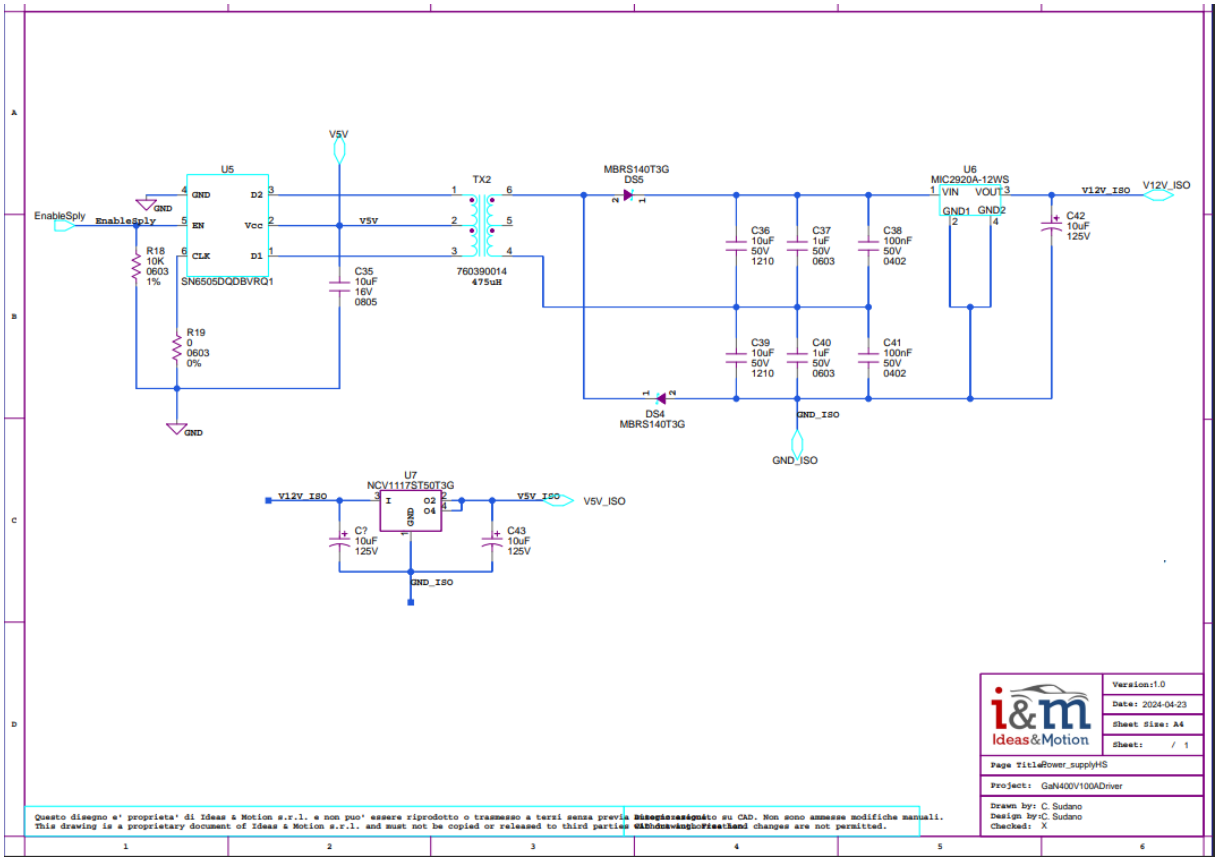


Figure 17: Schematic of isolated power supply

4.1.4 High-voltage monitor

For example, in high-performance GaN-based inverter designs using high-speed switching and high voltages, the High Voltage (HV) monitor is a safety component for the operational safety, performance and reliability. With efficiencies and switching speeds higher than their silicon-based equivalents, GaN

transistors need accurate voltage application and monitoring to ensure stable operation and to prevent damage through excessive voltages. A GaN-based inverter requires a high-voltage monitor to allow stable and safe operation of the final stage of power conversion, while constantly tracking high-voltage levels throughout key circuit nodes. Prevention of Voltage SpikesIn high-power systems, voltage spikes or ripples can be fatal to GaN transistors and other components. The HV monitor prevents these risks by detecting any overvoltage conditions and responding to them, which can otherwise result in component failure or gradual performance degradation over time.

The HV monitor also gives feedback to the control system to help adjust voltage as needed. To utilized the high performance and efficiency of GaN transistors as a quick-way regarding it within the GaN inverters,so need conflicting states for it to turning operation in GaN transistors. By allowing to provide accurate voltage data, the HV monitor also helps with thermal management; too much voltage can lead to increased power dissipation, which may cause thermal stress or runaway conditions. Now with the HV monitor, the inverter's control system is able to identify and act on potential problems before damage occurs, keeping the system within acceptable voltage and temperature ranges.

For the HV monitor of a GaN inverter some key components cooperate to enable precise, real-time voltage monitoring:

- High Voltage Isolation: the Inverter can have high voltages and the separation between high-voltage and low-voltage sides is key. Such isolation is enabled by components such as digital isolators or optocouplers that transfer signals across these domains while safeguarding low-voltage control circuitry. Isolation is critical to enable the safe operation of sensitive control in electronics applications. For this project, the selected digital isolator was the Skyworks Si8932D: this device is particularly ideal for its design to create a safe and reliable interface between high-voltage circuits and low-voltage control systems, in order to protect the measurement and control electronics from high-voltage transients and noise. The input range on the Si8932D is from 0 to 2.5 V [43].
- Voltage divider network: in order to efficiently process the high voltage appropriately, we implemented a resistive voltage divider network using ERJP series precision resistors. These resistors feature high precision and stability over a wide variety of temperatures and operating conditions, providing consistent measurement accuracy. Resistor value selection is critical to permetting the desired step-down ratio to satisfy the monitor, without degradation in accuracy at upper-range voltages. A voltage divider, adjusted with precise resistor values, scales down an initial

voltage of 450 V to the input specifications of the isolator. We employ for example three resistor of 150 kΩ for the isolator in series with a very accurate 2 kΩ one (tolerance of 0.1%) [44].

- Signal amplification with operational amplifier: the signal is being amplified with operational amplifier after stepping down the voltage with the divider to bring this into optimal range for control's circuitry. In this case, the op-amp shown in the schematic was the Texas Instrument OPA171, setup in a non-inverting configuration with a gain of 2; It provides a gain of 2 by making the two resistances equal on both the in- and output paths. In particular, resistors with value of 30 kΩ have been selected to guarantee steady and precise amplification.

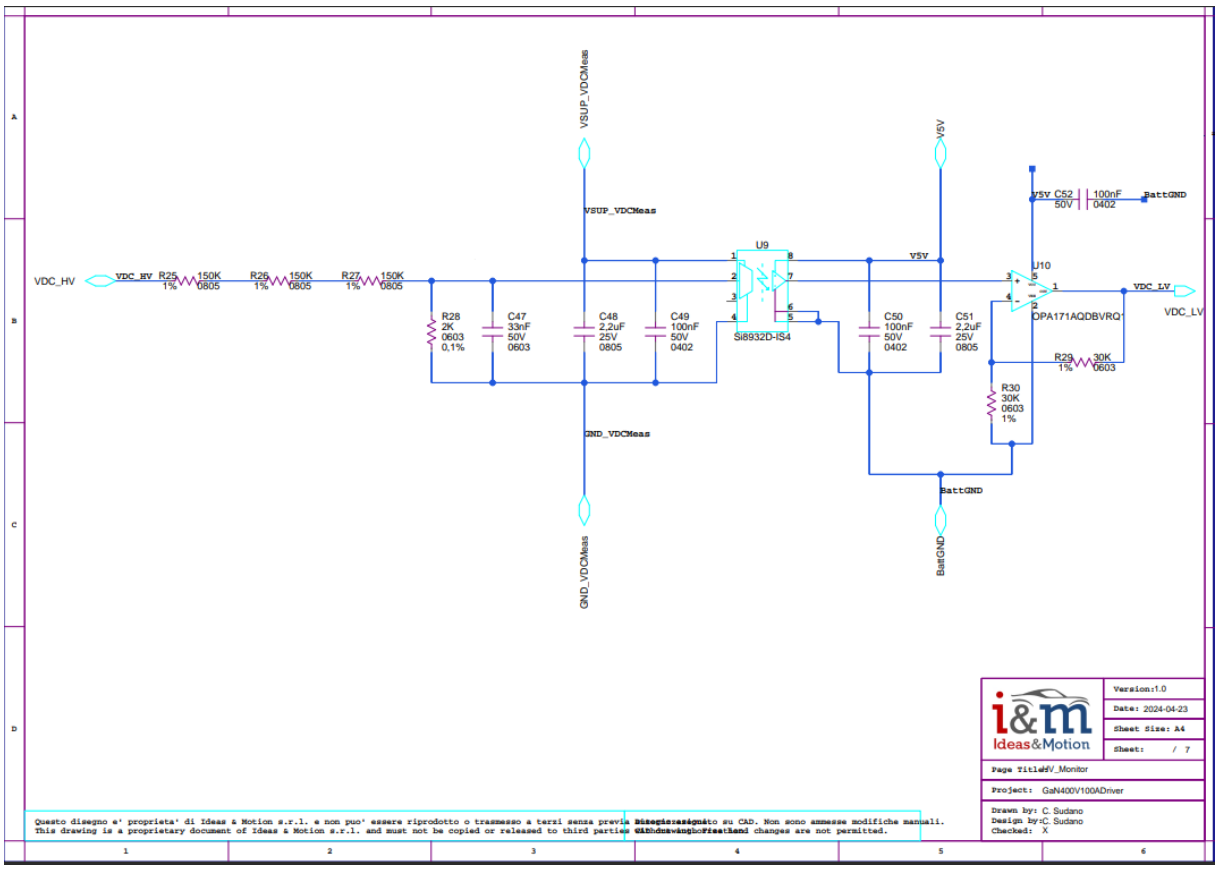


Figure 18: Schematic HV voltage monitor

4.1.5 Temperature monitor

Therefore, inverters and other high-power applications must control their operating temperatures in order to achieve system reliability, efficiency and longevity. Steady state performance can drop down as you reach hotter

temperatures, and thermal runaway can occur or in high voltages devices like GaN transistors, you may end up damaging the component permanently. The thermistor is a type of temperature-dependent resistor that changes its resistance according to the temperature. For this circuit, the thermistors are of the NTC (Negative Temperature Coefficient) type which means their resistance decreases with increase in temperature. What they permit is a defined response to changes in temperature, that may be read by the control system as the thermal condition of every point being monitored.

We utilize a special temperature circuit to monitor the critical temperatures in the inverter, wherein three thermistors are arranged to relay continuous feedback on various thermal points in our inverter system. The output from the thermistors corresponds to different parts of the inverter that need temperature monitoring:

- T_1: this output checks the transistors temperature. This measurement is critical because it involves the high switching frequencies and power levels handled by the GaN transistors. The balance between this output enables the system to monitor and respond to an increase in temperature at the transistors, which can cause either effective losses or damage if not managed.
- T_2: this signal is probably used to measure its DC link capacitor, which is certainly important for system voltage stabilization in the inverter circuit. Due to the frequent charge/discharge cycles on the DC link capacitor, an extreme thermal stress can be developed. This output provides temperature feedback that allows the system to protect the capacitor from damage through overheating, which could impact its efficiency or lifetime.
- T_3: this output monitors the temperature at the bypass circuit (an auxiliary/protection circuit of the system) Monitoring this temperature keeps the system stable and protected during the run.

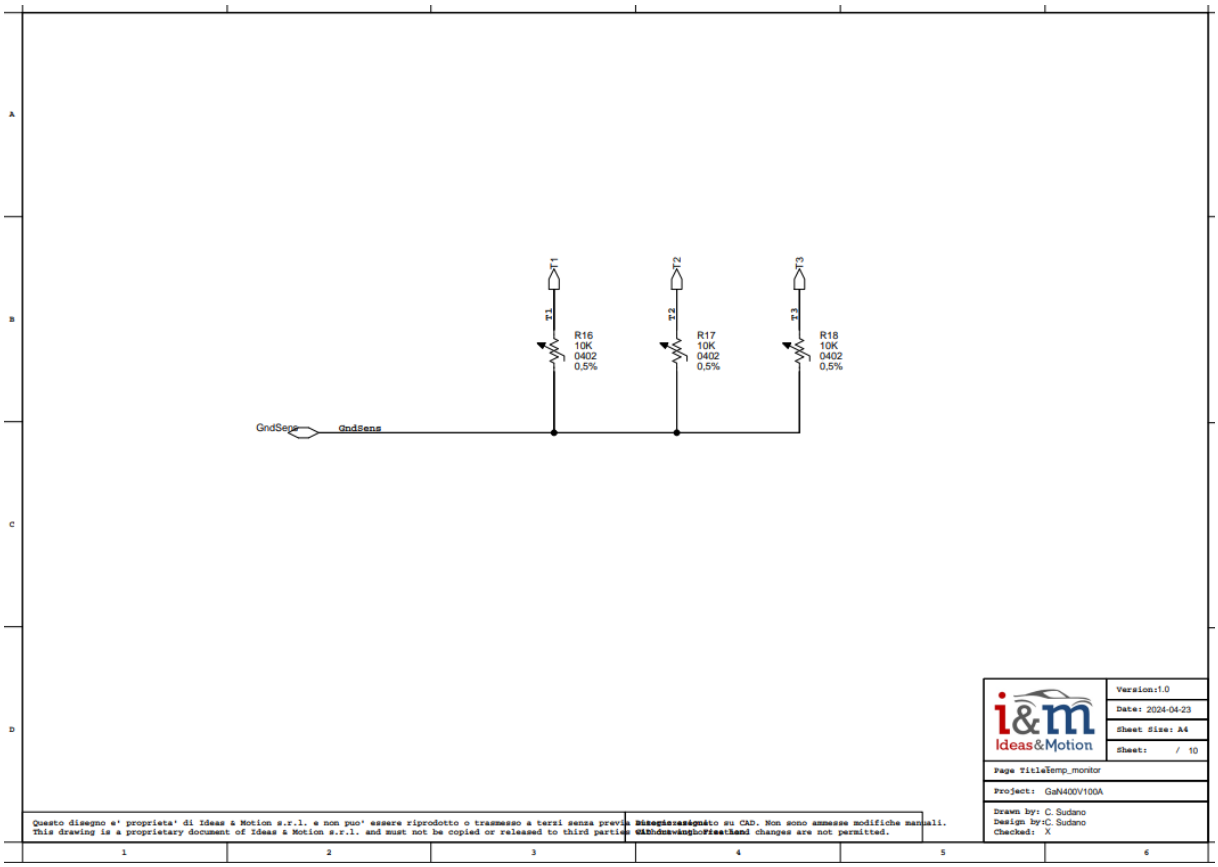


Figure 19: Schematic of temperature monitor

4.1.6 Current sensor

In power electronics, current sensing plays a key role in power electronics for the monitoring and control of the performance of various components, especially in high-power applications such as motor drives and inverters. Because this high precision is maintained, accurate current sensing enables feedback control that keeps the system operating within the required performance range. The sensor used in this project is the ACS37610, a high-accuracy current sensor based on Hall effect principles and integrated by Allegro Microsystems. The sensor is especially suitable for the high current ranges and provides high accuracy for applications such as inverters and motor drives. It works by measuring the magnetic field produced by the current that runs through a conductor. It detects current using the Hall-effect principle, meaning there is no direct electrical contact, improving isolation and safety in the system. The sensor produces an analog output signal which is proportional to the instantaneous current; this allows the control system to measure the real-time motor current.

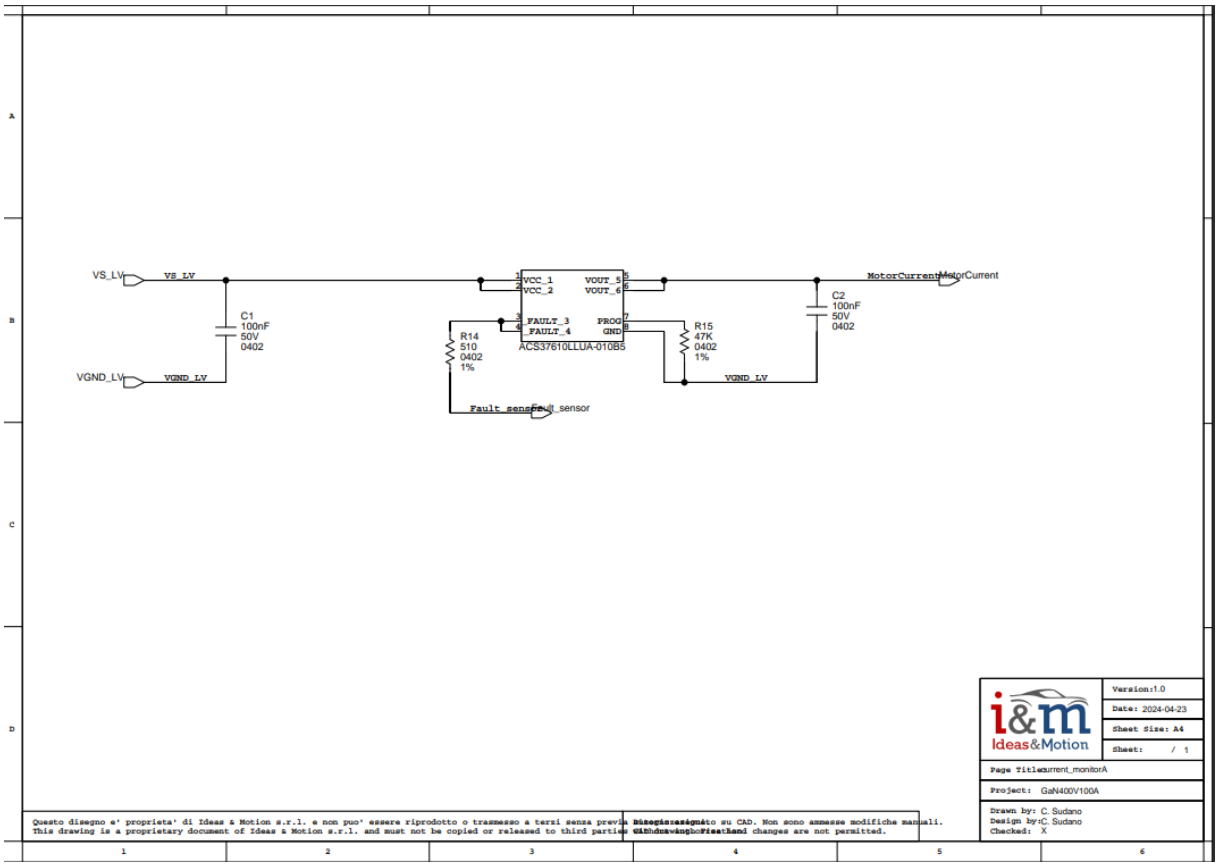


Figure 20: Schematic of current sensor

The ACS37610 includes a fault detection feature, which is activated when the current exceeds a predefined threshold. When this happens, the fault-sensor pin on each sensor generates a signal indicating an overcurrent condition. This fault signal is crucial for protecting the system from potential damage due to excessive current flow. Then, the fault signals from each sensor are connected together in a wired-OR configuration. These fault outputs are then pulled up to the supply voltage through a 100 kΩ pull-up resistor. This configuration means that if any one of the current sensors detect an overcurrent, it will pull the combined fault line low, triggering a system-wide FAULT signal [45].

Chapter 5

Testing

Testing represents a crucial step in the lifecycle of power electronics systems as it constitutes the link between the design and the field deployment. Testing is a crucial aspect of this project as it ensures that the system behave as designed and that it can work correctly under a range of operating conditions.

This chapter outlines the approached methods and procedures that were followed for the functional verification of the GaN-based power stage at variable current and voltage, the experimental setup, as well as the extensive measurements and discussion for the different obtained results.

5.1 Double-Pulse Test

When correctly dimensioned and cooled, power devices may safely carry nominal current (while in the ON state) or withhold nominal breakdown voltage (while in the OFF state). These components, however, need to be turned ON and OFF several times per second and in those very transitions, they undergo life-threatening stress due to stray inductances existing in the commutation path.

The flow path is the route of components (real and parasitic) that the current follows when a switch is commuted. This definition is important because it indicates what enters into the analysis, allowing us to focus only on those parts which play an active part in the process of commutation.

The characteristics of turn-on and turn-off of a power switch act like any other switch except for the current being switched and the voltage applied. Two important features of these switching operations however makes them prone to challenges:

- Stray inductances in the commutation paths which tend to be large, due to large power components (transistors, diodes, capacitors) and due to required clearance and creepage distances to prevent arcing.
- Fast switching times are required to reduce energy losses and increase phase margin for better controllability on the output side.

The combination of these factors results in a rapid voltage rise at the terminals of the power components, which is harmful.

To allow the evaluation of the switching behaviour at different current levels, the double-pulse test was developed. The idea is to saturate the current through the circuit by turning on a DC voltage across an inductive load for a specified amount of time. When the desired current level is achieved, the transistor under test is turned OFF and ON to monitor its performance.

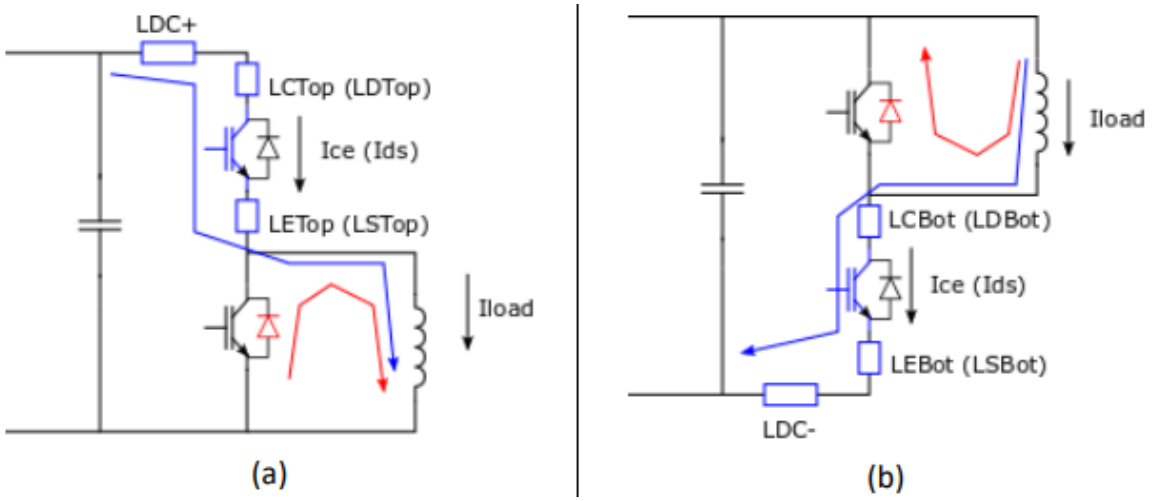


Figure 21: Electrical connection for DPT

The two configurations typically described in literature for double-pulse tests of a two-level voltage source inverter are shown in Figure 21. In these arrangements, one inductor is placed as load in between single phase and DC terminal. Switching the transistor under test ON and OFF makes the current flow alternately through the transistor, and subsequently through the anti-series diode. This process mimics standard commutation in case of inverter working, and gives an insight about stray inductancies in commutation path that stresses out the system. This test requires closely controlling the gate driving of transistor, as well as monitoring the current and voltage at its high-voltage terminals.

The test focuses on the low side GaN FET and the freewheeling (FW) diode of the top one, which can be done over all three inverter phases or, if required, on only selected ones. It applies a sequence of a long pulse, a shorter pulse and a desired time between them to the gate of the bottom transistor. Short circuiting the top GaN FET gate to source ensures that the upper GaN FET remains OFF and lets the FW diode be tested. The self-connected coil circuit can be seen as an inductor connected between the drain and source terminals of the upper diode. The process consists of three key steps:

- First Long Pulse: the bottom transistor is switched ON from a near-quiescent state, and the inductor is connected to the DC link voltage, therefore provoking a linear current ramp-up. During this stage, the current also flows through the bottom GaN FET. (The goal here is to know the turn-off time and the energy dissipated in that transition.)
- Intermediate OFF Period: The transistor is turned OFF when the current through the inductor reaches the desired value. As the inductor tries to keep its current constant, the current path changes through the FW diode. Next, during this time, the bottom GaN FET drain-source voltage will elevate and will saturate immediately at the value equal to DC link voltage + the overvoltage provided by third term in Form 4 (the current being switch off has to be multiplied by stray inductance and divided by switching time). Once this value is hit, the voltage switches back to the DC link voltage
- End Short Pulse: bottom transistor is turned ON yet again; voltage across collapses to its saturation value. The load effectively sets the transistor current much more quickly than if the transistor were to be held off, waiting for a turn on the FW(D) diode in reverse recovery. After reverse recovery is finished, diode returns to OFF state and the inductor integrates voltage on its terminal which raises the current through it. This phase is meant to test the time taken to turn-on the GaN FET, monitor the reverse recovery current of the body diode and measure the energy lost in the turn-on event [46].-

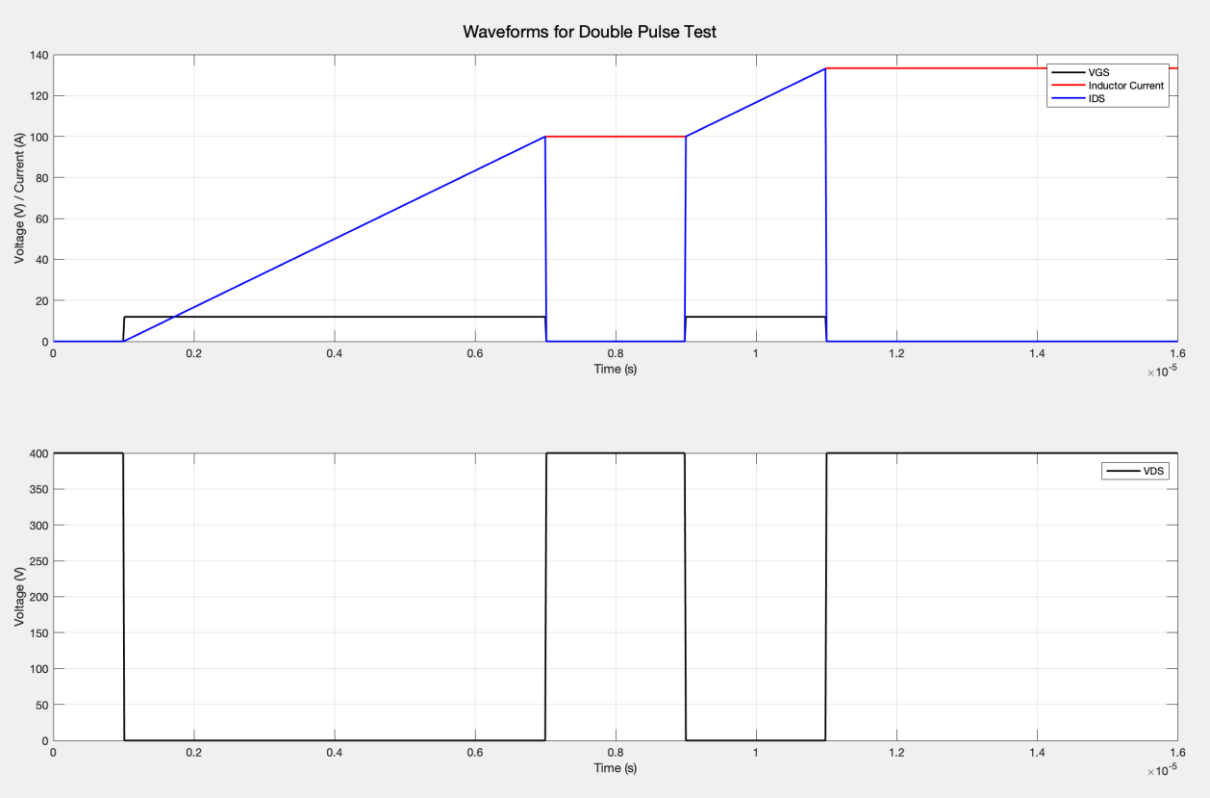


Figure 22: Waveforms to be monitored during the test

For this test, precise and reliable instrumentation is essential to ensure accurate measurement and safe operation. The first component we need is a high voltage power supplier capable of reaching at least the DC voltage used for the circuit in use. Then a high-bandwidth, four-channel oscilloscope is essential for this setup, allowing for the simultaneous capture of critical waveforms such as the drain-source voltage, gate-source voltage and current through the device under test. The oscilloscope should have a bandwidth sufficient to accurately track high-frequency switching events. The final piece of laboratory equipment is the arbitrary waveform generator (AWG). This device needs to be highly versatile as it is responsible for generating two separate pulses: the first pulse is used to load the inductor to the required current level, while the second pulse, which has a fixed width, is used to switch the transistor ON and OFF. If an AWG is not available, a properly interfaced microcontroller can be used as an alternative to control the gate driver. In this application a control board is used, instead of a waveform generator, to drive the gate driver. The control board is operated via a PC using the CAN protocol, which ensures robust and reliable communication. The use of a control board in place an AWG offers enhanced flexibility and precision, allowing for the implementation of complex control strategies and real-time adjustments.

As outlined in earlier sections, it is crucial to precisely monitor several parameters during this test, such as gate voltage, voltage at the drain-source terminals and current passing through the inductor. The first two voltages are typically floating with respect to the oscilloscope, so it is highly recommended to use differential probes for each measurement. These probes should be capable of handling at least double the maximum DC voltage present in the circuit, as the voltage range typically matches that of the inverter. The current that needs to be measured should span the entire range that the system will operate within. Specifically, Rogowski probes are recommended due to their compact size and ability to fit around terminal they have to monitor. The test involved reaching 500 V and 150 A: these values are harmful to the human body and also permanently damage components. For these reasons, the testing bench is covered with a plexiglass box to avoid direct contact or risk of flying debris in case of component damage. It is also important to discharge the input capacitors with the help of resistors after the test is performed.

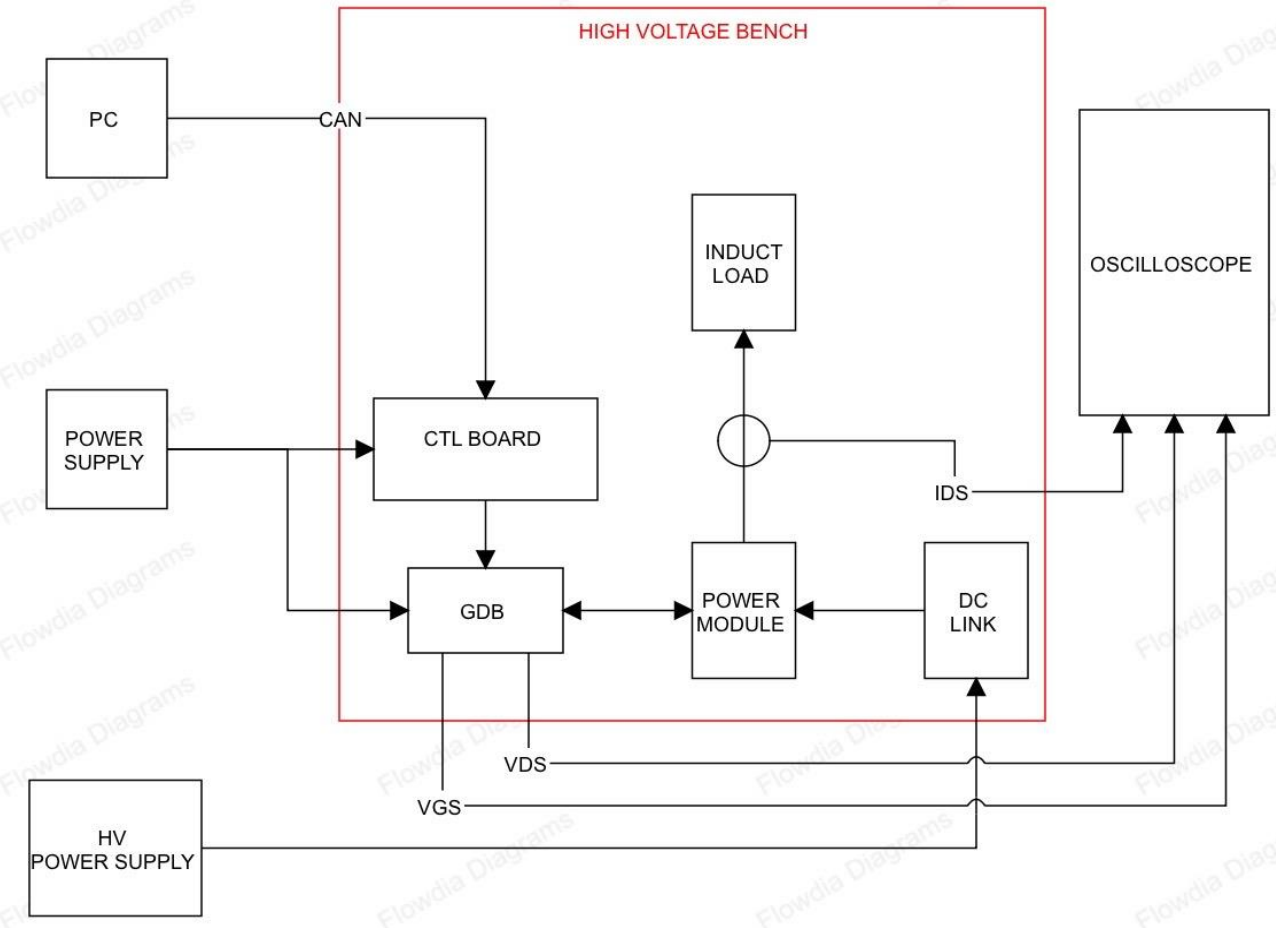


Figure 23: Diagram of laboratory setup for the test

Therefore, instrumentation comprehends:

- EA-PS9500-30 3U High Voltage DC Power Supply. It is employed to generate voltage up to 500 V.
- CPX400DP. It is employed to generate 40 V to supplies the control board and 12 V for the gate driver board.
- LeCroy AP031: measures gate-source voltage.
- Rohde & Schwarz RT-ZD01: measures drain-source voltage.
- PEM CWT UM/6/B/1/80 AC Rogowski Current Probe: measures current flowing through the inductor.
- LeCroy HDO9104 Oscilloscope (1 GHz). Four channel to display all measured waveforms.
    1. Channel 1 (yellow): displays the power ($V_{DS} \times I_{DS}$).
    2. Channel 2 (purple): displays drain-source current.
    3. Channel 3 (blue): displays gate-source voltage.
    4. Channel 4 (green): displays drain-source voltage.

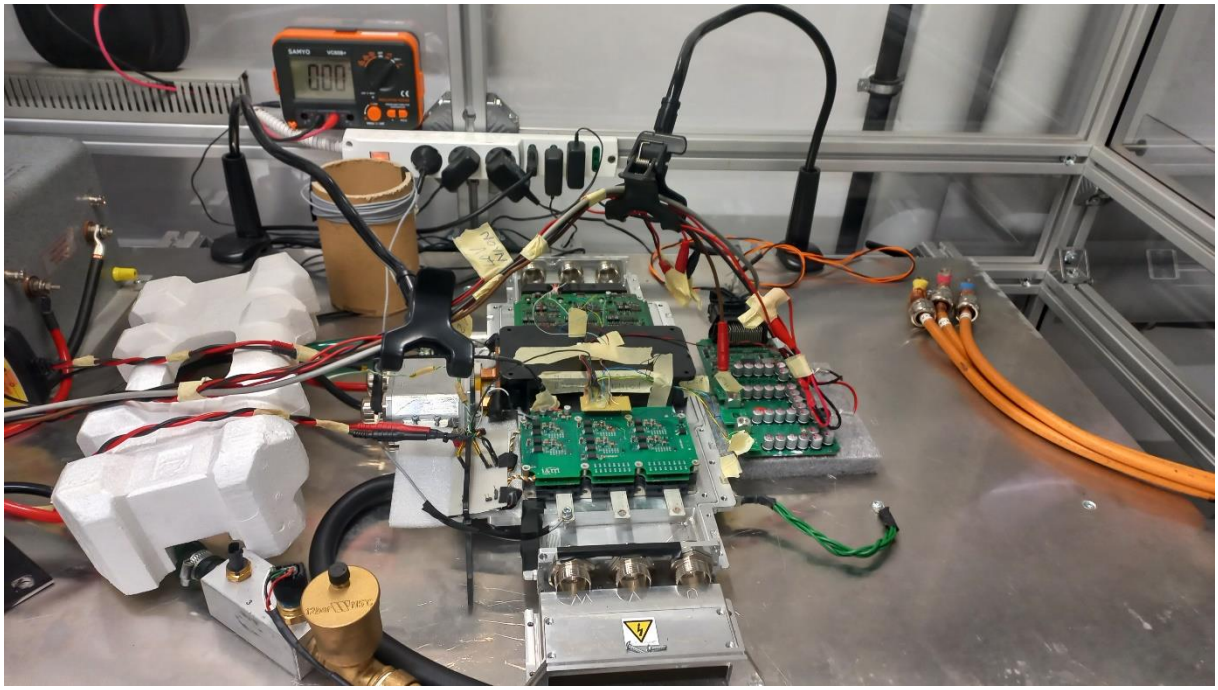


Figure 24: Laboratory setup

The primary objective of this test is not to quantify losses or observe current spikes caused by the reverse recovery of the body diode. Such information is

typically provided by the manufacturer under the specified operating conditions. Instead, the main focus is to ensure that the inverter operates as intended, delivering waveforms that align with the desired specifications. Additionally, the test serves to assess turn-on and turn-off timings to accurately configure the dead-band within the modulation block.

This test specifically targets the bottom switch in inverter leg 1, as it is deemed adequate for this purpose. It is worth noting that the current passing through the bottom transistor cannot be measured directly due to the absence of access to the gate driver and inverter system. In this work, results are presented and analyzed for the DPT conducted with V_{DC} of 300 V, 400 V, 500V and I_{DS} levels of 25 A, 60 A, 100 A and 150 A.

Figure 25, 26, 27 and 28 shows the captured form when V_{DC} is 300 V at different current levels

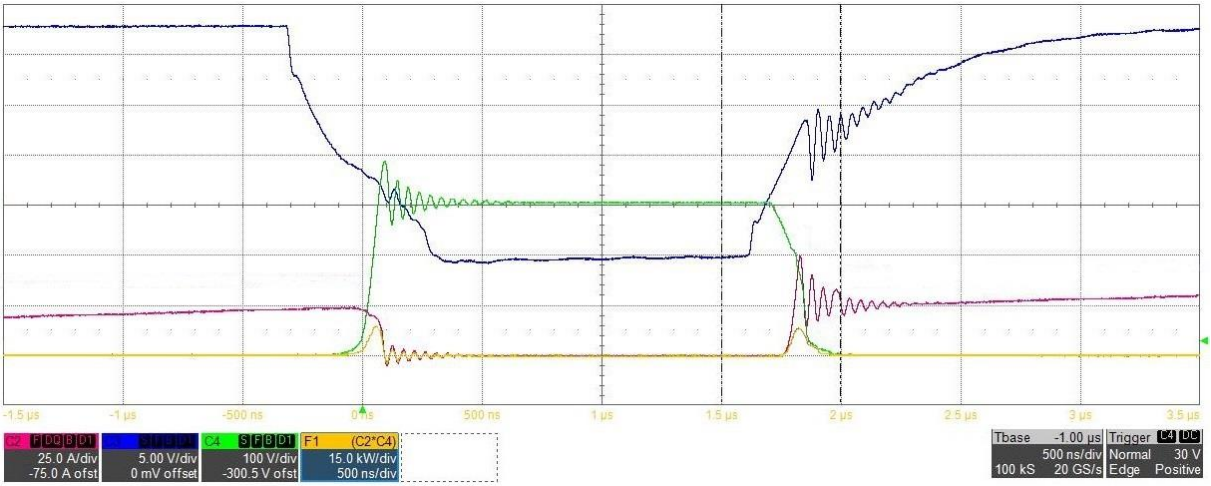


Figure 25: DPT waveforms with V_{DC}=300 V (green) and I_{DS}=25 A (pink)

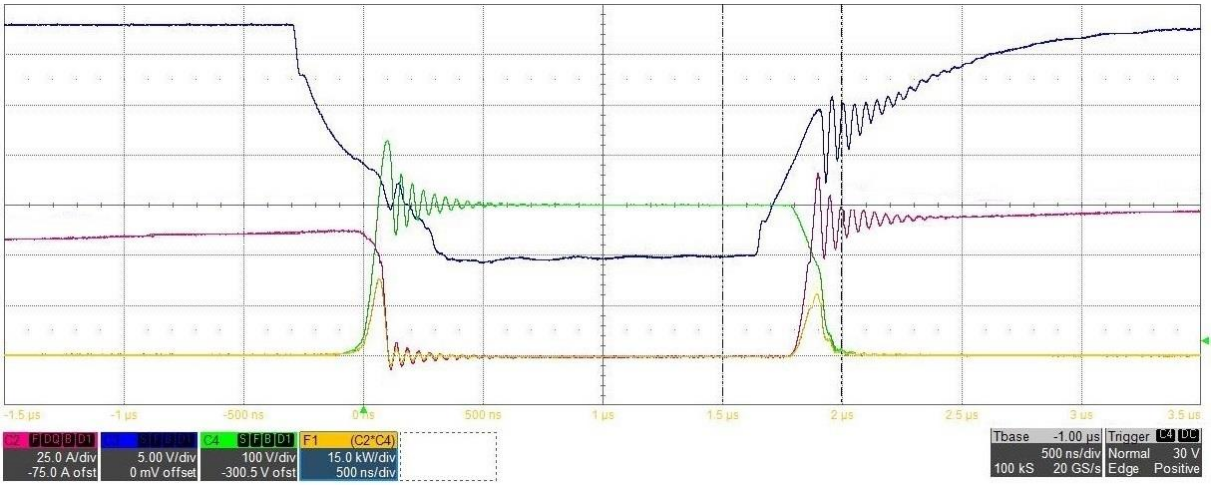


Figure 26: DPT waveforms with V_{DC}=300 V (green) and I_{DS}=60 A (pink)

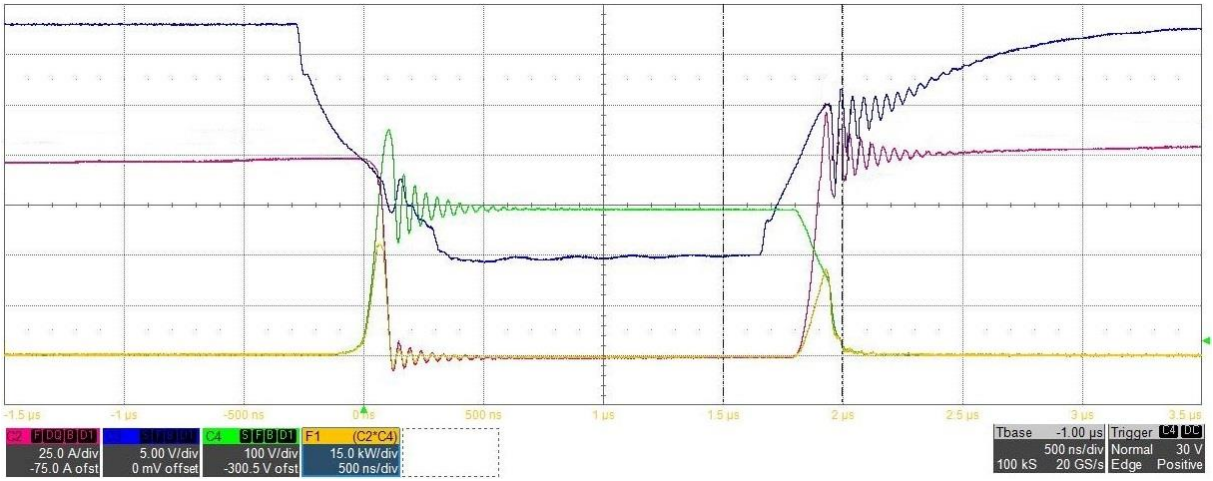


Figure 27: DPT waveforms with V_{DC}=300 V (green) and I_{DS}=100 A (pink)

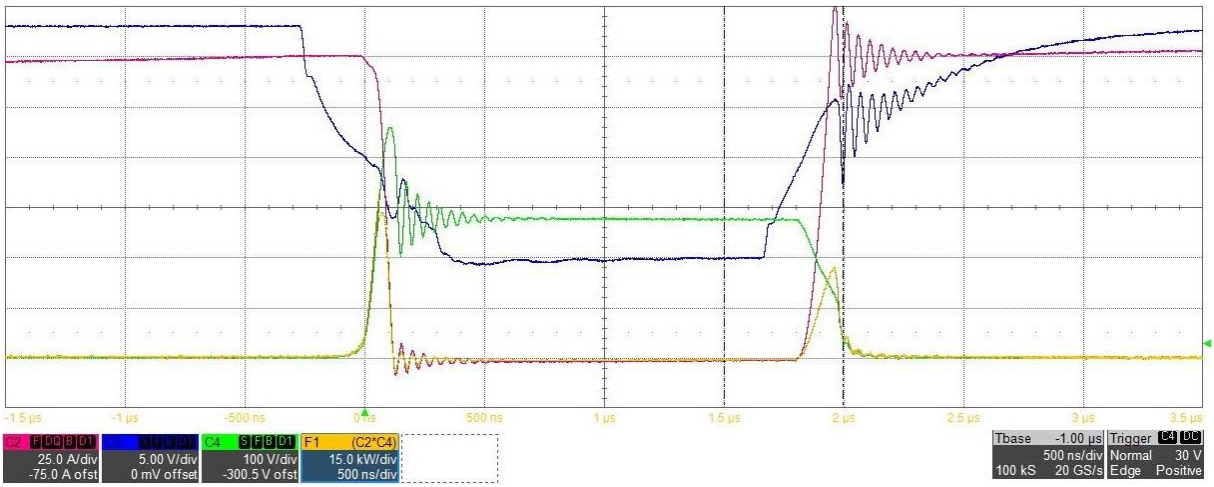


Figure 28: DPT waveforms with V_{DC}=300 V (green) and I_{DS}=150 A (pink)

The Double-pulse test measurements successfully confirmed the correct operation of the circuit, ensuring that the observed waveforms matched the expected behaviour. In addition, this test provides quantitative data for evaluating key parameters that influence operation of the inverter. Using the results obtained, we can now analyse how critical parameters such as overvoltage, switching inductance and switching energy behave as a function of operating variables like V_{DS} and I_{DS}.

- **Energy (E_{on} and E_{off}) vs I_{DS} and V_{DS}**

Switching energy was calculated by intergrating the instantaneous power over the switching intervals:

$$E_{on/off} = \int_{t_{on/off}} I_{DS} V_{DS} \, dt \qquad (25)$$

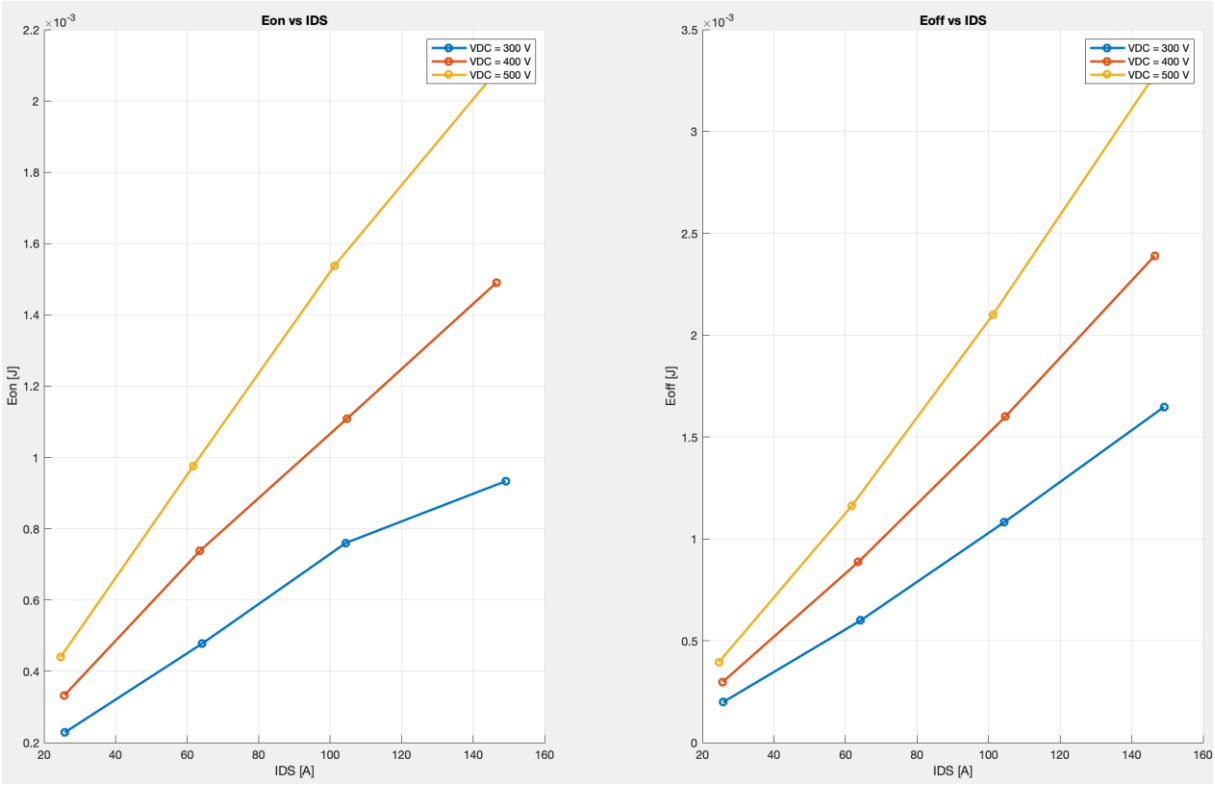


Figure 29: Energy vs I_{DS}

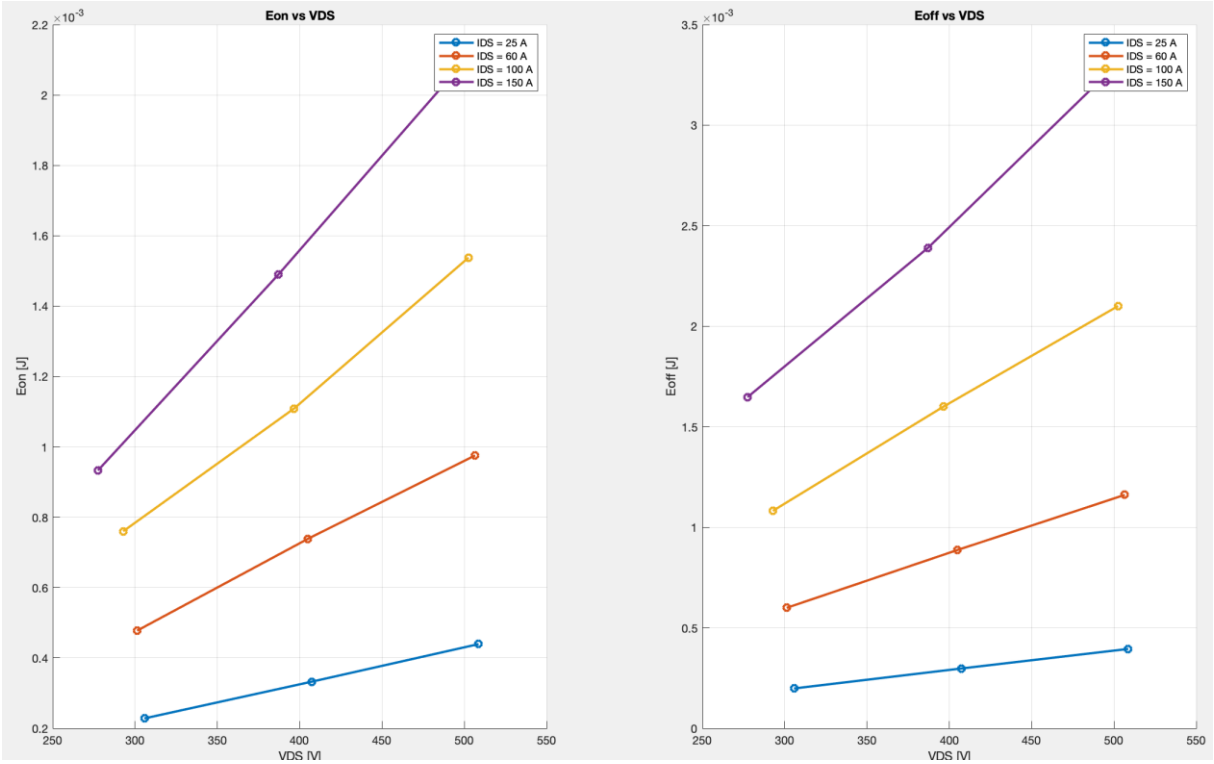


Figure 30: Energy vs V_{DS}

As expected, the turn-on energy increase linearly with increased current I_{DS}, as shown in the left chart of the figure y. This trend can be attributed to the resistive losses during the current ramp-up phase and the additional energy needed to overcome the inductive effects of the circuit. At higher I_{DS}, the energy stored in the inductive load is greater, leading to a higher E_{on}. On the other hand E_{OFF} are lower at low currents but rise significantly at higher currents. Results are good enough for hard-switching since E_{oss} is dissipated at turn-on.

The Figure 30 shows that both Energy increase linearly with V_{DS} for al tested drain current levels. This behaviour align with theoretical expectations and datasheet specifications.

The measured values for the turn-on and turn-off energies, as well as the associated losses, align well with the specifications provided in the datasheet of the power module. This consistency confirms the accuracy of the experimental setup and the reliability of the device under the tested conditions.

- **Overvoltage vs I_{DS} and V_{DS}**

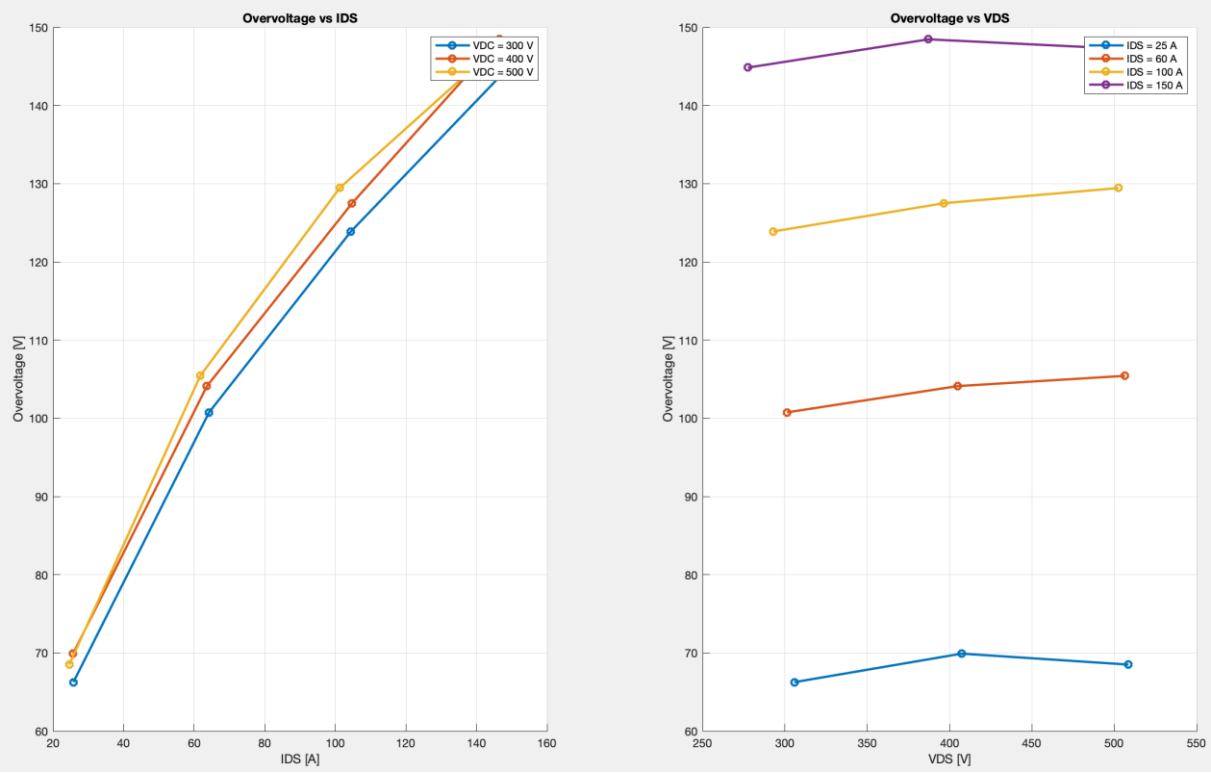


Figure 31: Overvoltage vs VDS and vs IDS

The overvoltage peak occurs during the turn-off transition due to the stored energy in the circuit's stray inductance:

$$V_{peak} = V_{DS} + L \cdot \frac{di}{dt} \tag{26}$$

The left chart of the figure 31 indicates a nearly linear increase in overvoltage with $I_{DS.}$ Higher currents result in larger energy release during turn-off, amplifying V_{peak}. The impact is more prominent for higher V_{DC}. The right chart, instead, indicates that overvoltage slightly increases with V_{DC} but stabilizes beyond 400 V for higher currents. This behaviour suggests an interaction between the device parasitics and the external circuit.

- **Stray Inductance vs I_{DS} and V_{DS}**

The commutation inductance was derived by analysing the relationship between overvoltage and the current derivative respect to time:

$$L = \frac{V_{peak} - V_{DS}}{\frac{di}{dt}} \tag{27}$$

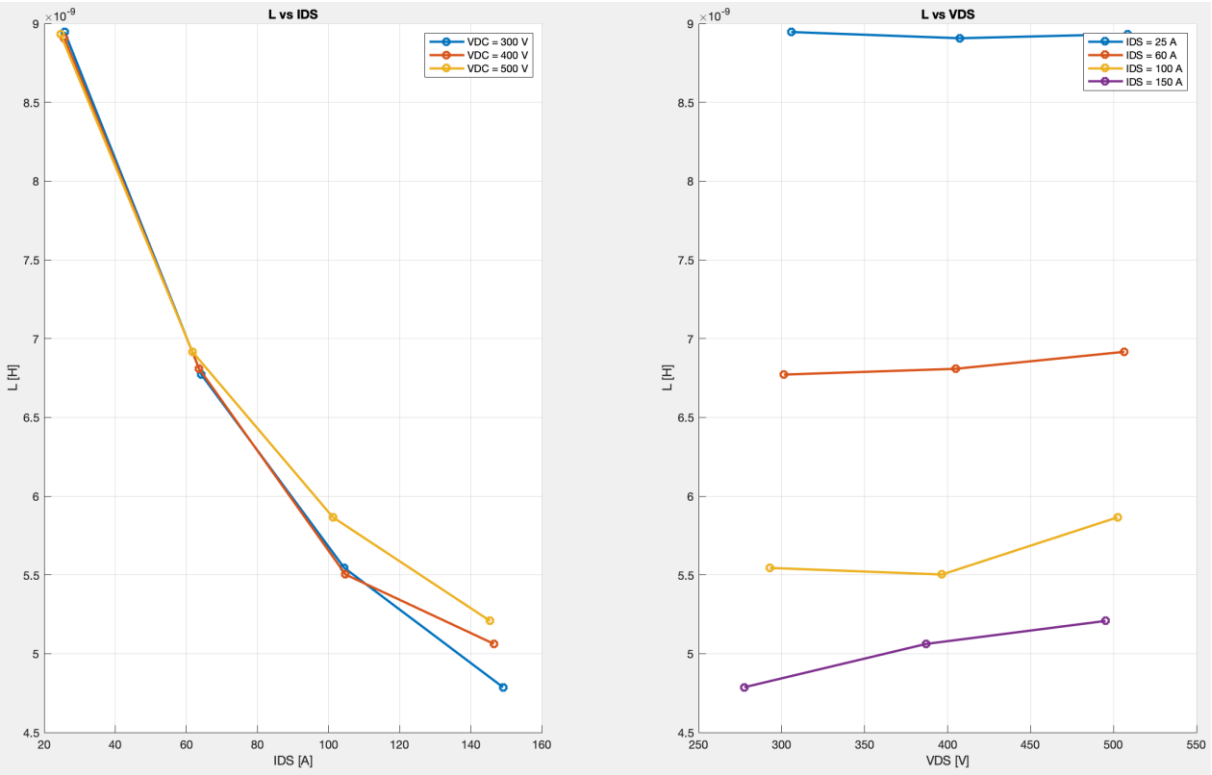


Figure 32: Stray Inductance vs VDS and vs IDS

A clear reduction in L with increasing I_{DS} suggests saturation effects in the circuit and reduced parasitic influence. L is relatively stable across V_{DC} levels, indicating that the stray inductance is more influenced by circuit geometry than operating voltage.

In conclusion, the Double-Pulse test results confirm that the switching dynamics of the tested GaN devices behave as expected. This analysis provides a solid foundation for further design optimization, ensuring efficient and reliable operation in automotive and high-power applications.

Chapter 6

Conclusion

This thesis has presented the design and characterization of a modular power stage based on Gallium Nitride (GaN) devices, aimed at advancing the performance of automotive inverter applications. The integration of wide-bandgap (WBG) semiconductor technology has enabled significant achievements in efficiency, compactness and power density, addressing the demanding requirements of modern power electronics systems.

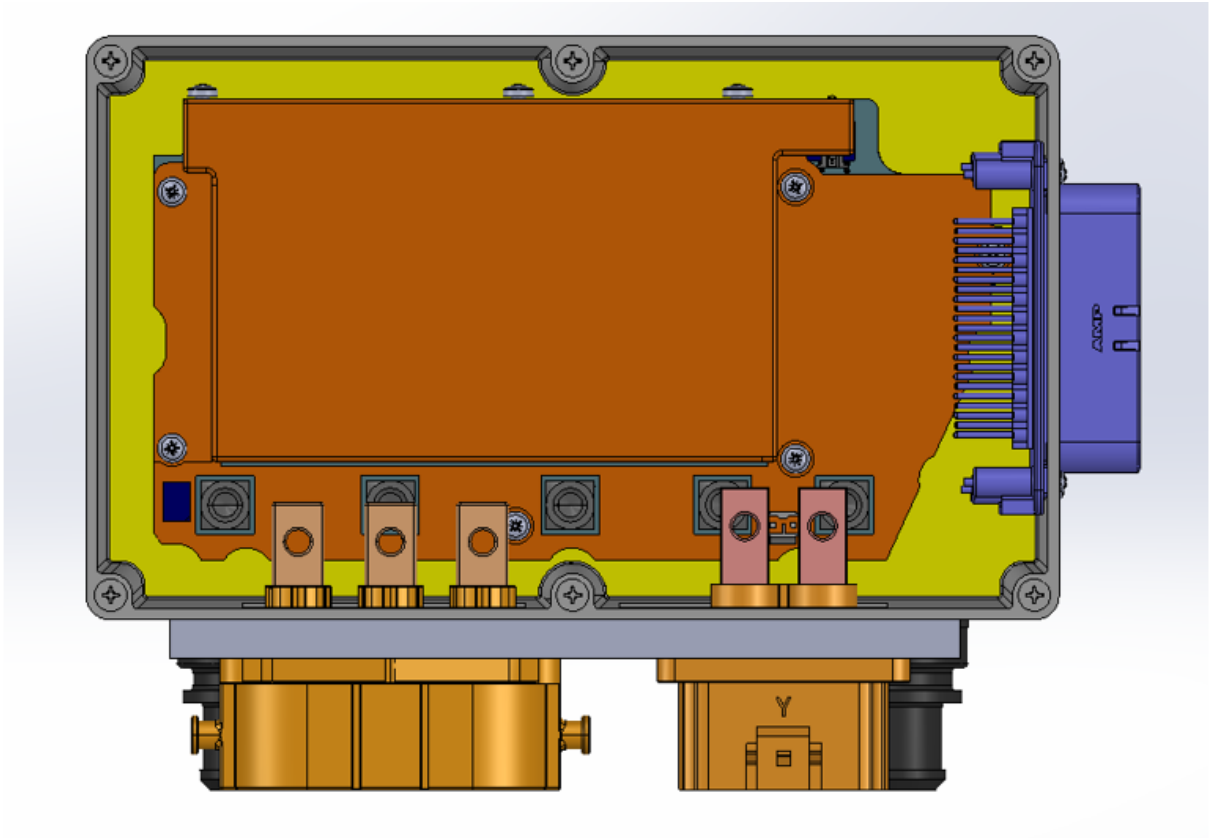


Figure 33: Internal view of the GaN-based inverter developed in this work

The inverter was developed in this study showed excellent performance, with a device weighing only 603 g, and a total volume of 2 l (0.4 l without the enclosure). These sorts of accomplishments align nicely with recent trends in inverter technology, where the pitch has rolled to high power density, low weight and

efficiency requirements of modern applications like electric vehicles and renewable energy systems. Thanks to the high switching speed, low losses and great thermal stability of GaN transistors, it was possible to implement a modularised three-phase structure, with the capacity to work to a nominal voltage of 400V and currents up to 150A per phase.

Various tests such as the Double Pulse Test helped validate the performance of the inverter by providing detailed information about switching losses, overvoltage and commutation inductance. These measurements confirmed expected trends and agreed well with theory, showcasing the benefits for high voltage and current operation of GaN-based designs. The automotive inverter used in the study was proven capable of fulfilling these performance requirements, which have extremely high reliability and efficiency in automotive applications.

Overall, this work has validated that GaN-moving inverters can be tailored to meet and better address the demanding requirements of modern KPIs, establishing their potential to be an enabler in the electrification of transportation. Aside from realizing the goals of the work, this leaves space for further innovation. Future investigations can focus on coupling the inverter with a complete powertrain to assess its system-level performance, developing advanced control algorithms for improved dynamic response, as well as investigating novel thermal management solutions to further enable power density improvements. It can thus be considered as a piece in the puzzle for the upcoming wide-bandgap technology adoption moving towards compact and efficient energy solutions for future applications.

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